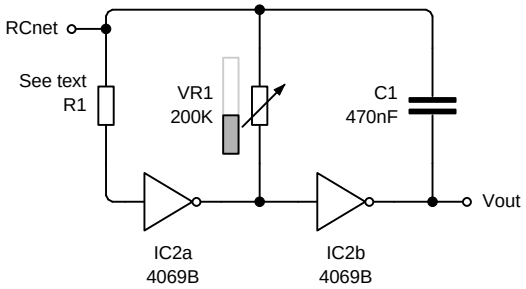
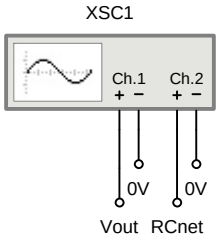
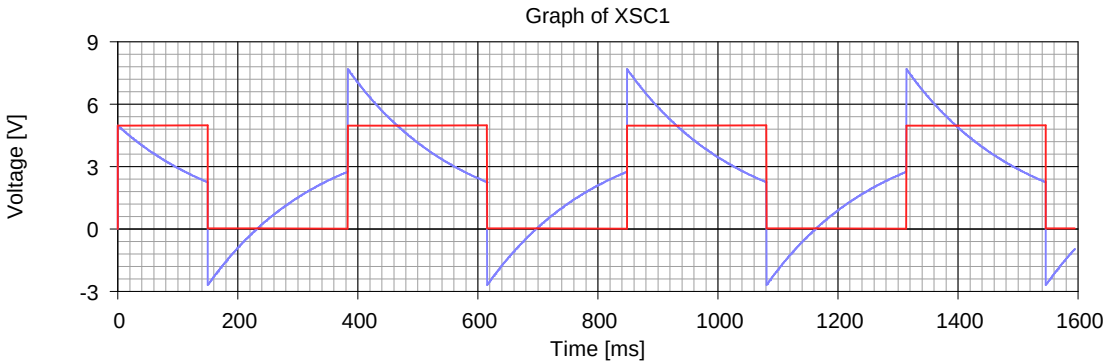
NOT GATE ASTABLE

This astable is based around just 2 logic gates. It is a classic example of a logic gate astable. Any inverting gate can be used in place of the NOT gates.

R1 is not always necessary and depends on the type of gates you are using. I have found it always functions correctly with the resistor included so continue to do so when designing circuits. A suitable value is 1K.







Circuit Explanation
(take this slowly and refer to circuit and traces on graph)

Assume the input to the first gate, IC1a, is low. Its output will therefore be high, and thus "Vout" (red trace) will be low. C1 will start to charge up through VR1, from the high output of IC1,. (blue trace "RCnet"). When the capacitor reaches 2.5v, the NOT gate (IC1a) now sees the input as a high input, thus sending its output low. This in turn causes IC1b to flip sending Vout high.

Now the gates have all inverted. The input to the first gate, IC1a is now high, thus its output is low and Vout is high - this is the "mark" state (the "on" part of the cycle).

As soon as this happens, "RCnet" now effectively is at 7.5 volts. This is because the output of IC1b is high, +5v and the capacitor has 2.5v in it still.Since these voltages are in series and of the same polarity they are added together, +5 + +2.5v = +7.5v.

Instantly the capacitor starts to discharge since the charge path in now reversed - all gates have flipped. As the capacitor empties out, it begins to charge with an opposite polarity, since gates are now inverted. When it charges to -2.5, the voltage at "RCnet" reaches and falls below +2.5v (+5v + -2.5v), IC1a now sees this input as a low input and inverts the output high. In turn Vout then goes low.

Now the gates are back as they were orginally. The voltage at "RCnet" is now -2.5v. (0v + -2.5v). The capacitor begins discharging until empty. Then the process repeats with a positive charge building in the capacitor.

(note positive and negative terms regarding charge are in relation to "Vout" and indicate charging polarity, to demonstrate the addition and subtraction of voltages, with and against the output voltage.)