



HCF4521B

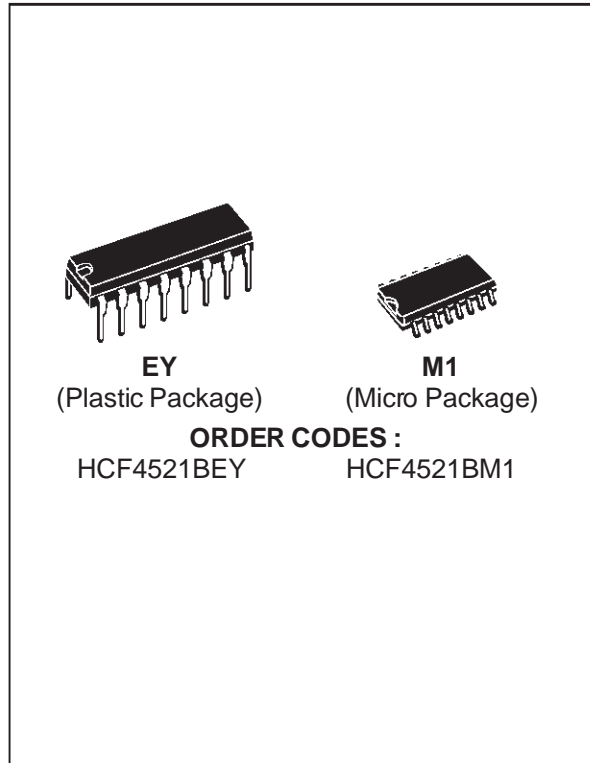
24 STAGE FREQUENCY DIVIDER

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- VOLTAGE SUPPLY RANGE 3V TO 18V
- ALL STAGES ARE RESETTABLE
- RESET DISABLES THE RC OSCILLATOR FOR LOW STANDBY POWER DRAIN
- RC AND CRYSTAL OSCILLATOR OUTPUT ARE CAPABLE OF DRIVING EXTERNAL LOADS

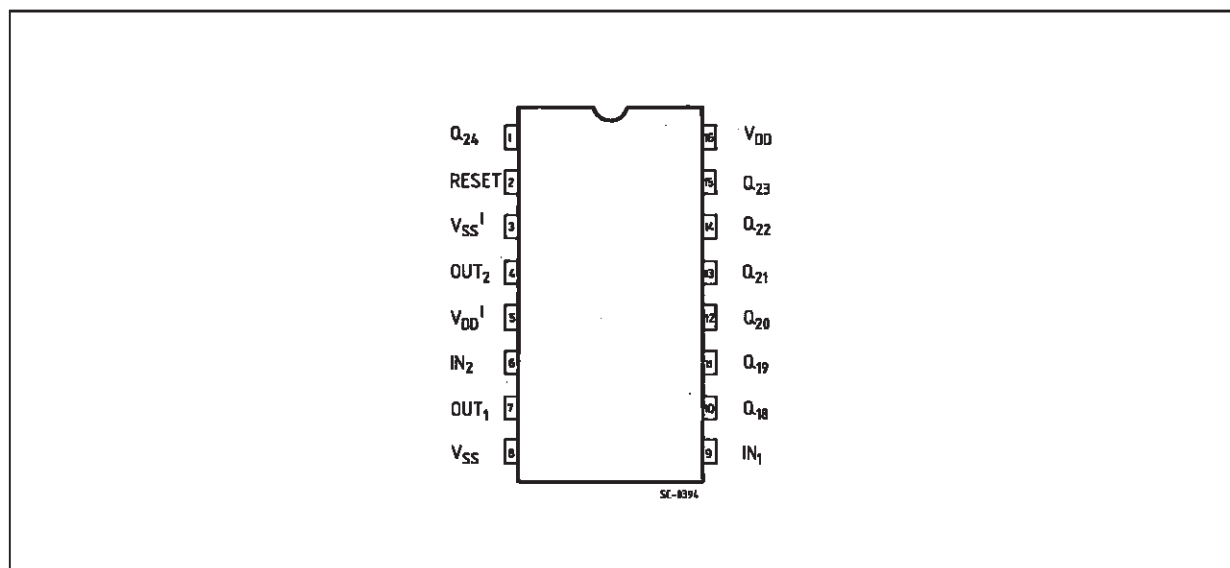
DESCRIPTION

The HCF4521B is a monolithic integrated circuit, available in 16-lead dual-in-line plastic package and plastic micro packages.

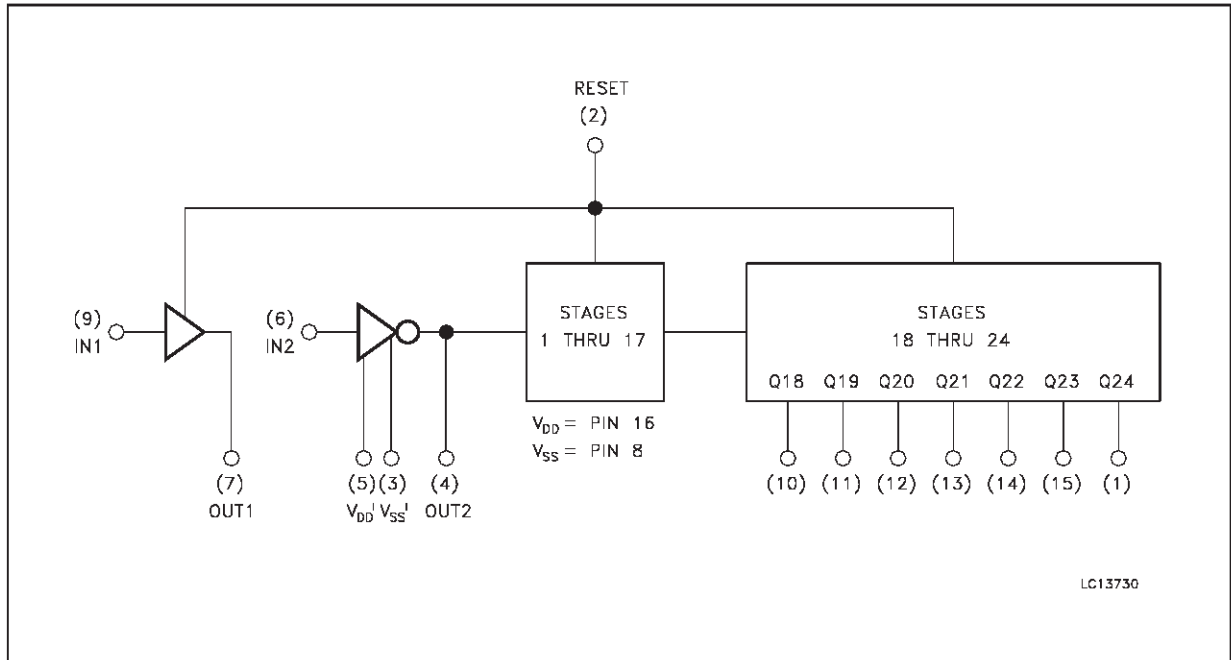
The HCF4521B have a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input circuit functions as a crystal or an RC oscillator or as an input buffer for an external oscillator. Each flip-flop performs a divide-by-two function giving a total count of $2^{24} = 16,777,216$. The count advances on the negative going edge of the clock. Access is available to the final seven stages giving the device added flexibility.



PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}^*	Supply Voltage	-0.5 to +18	V
V_i	Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_i	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package)	200	mW
	Dissipation per Output Transistor for T_{op} = Full Package Temperature Range	100	mW
T_{op}	Operating Temperature	-40 to +85	$^{\circ}C$
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

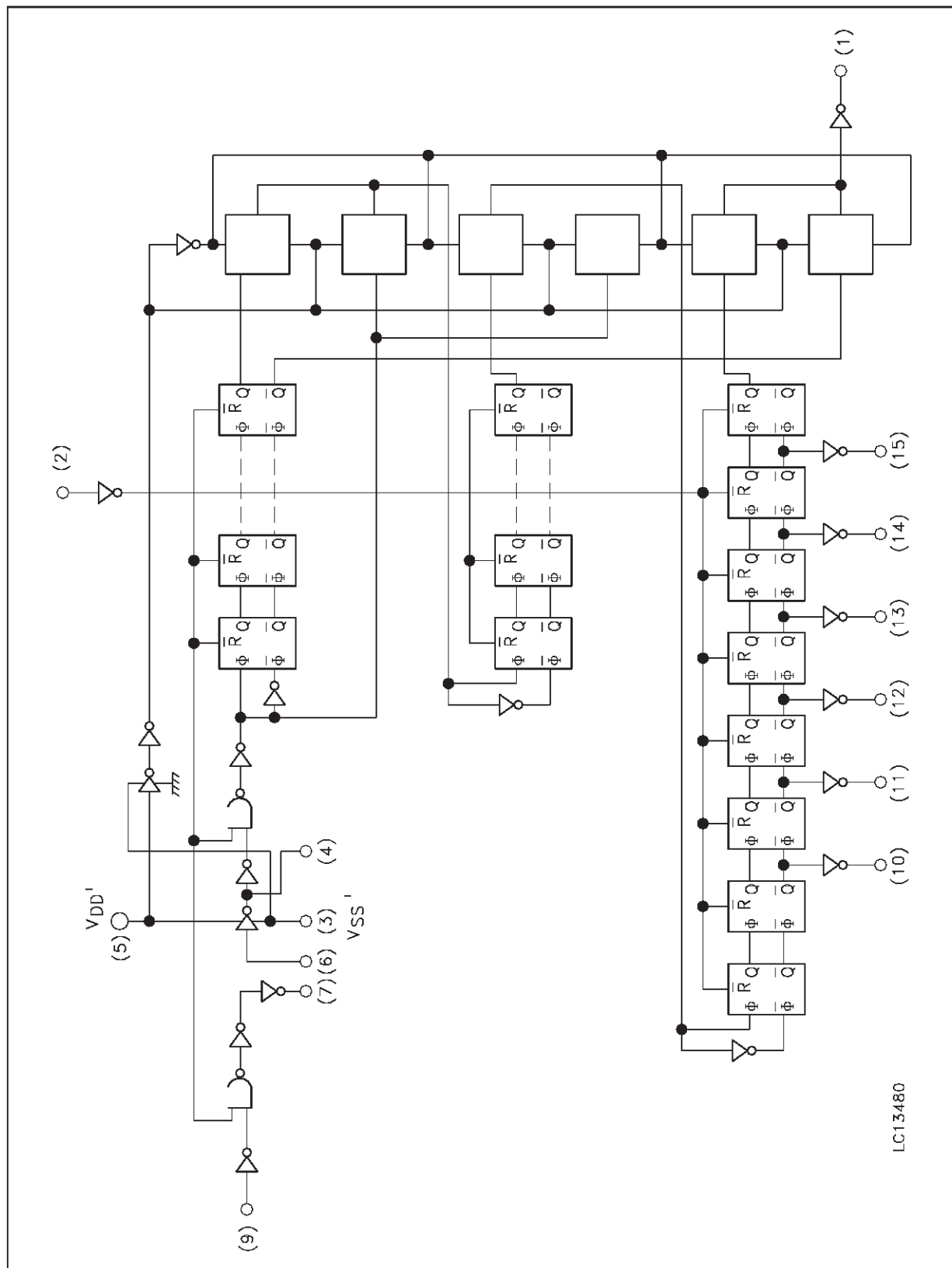
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 15	V
V_i	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-40 to +85	$^{\circ}C$

FUNCTIONAL DIAGRAM



LC13480

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions, voltages
References to V_{SS})

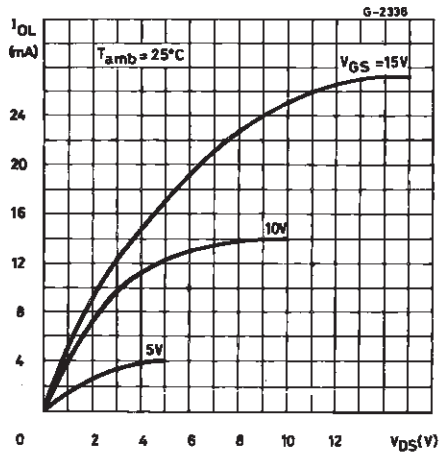
Symbol	Parameter	Test Conditions				Value						Unit	
		V_I (V)	V_O (V)	$ I_O $ (μA)	V_{DD} (V)	-40 °C		25 °C			85 °C		
						Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I_L	Quiescent Current	0/5			5		20		0.04	20		150	μA
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		mA
		0/5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
		0/15	13.5		15	-3.5		-3.0	-6.8		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.52		0.44	1		0.36		mA
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_i	Input Capacitance		Any Input					5	7.5				pF

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD} = 5V$, 2V min. with $V_{DD} = 10V$, 2.5V min. with $V_{DD} = 15V$

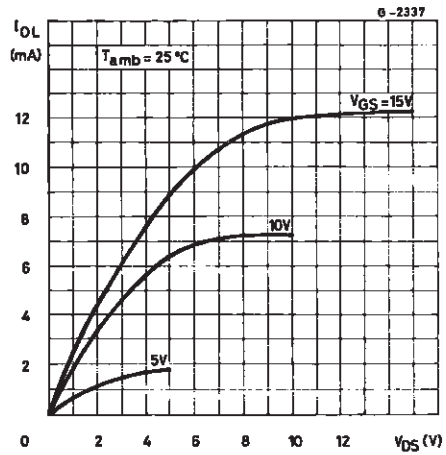
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$, typical temperature coefficient for all V_{DD} values is $03\text{ }^{\circ}\text{C}$, all input rise and fall times = 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}	Output Rise Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{PHL}	Output Fall Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q18		5		4.5	9.0	μs
			10		1.7	3.5	
			15		1.3	2.7	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q24		5		6.0	12	μs
			10		2.2	4.5	
			15		1.7	3.5	
t_{PHL}	Propagation Delay Time RESET to Qn		5		1300	2600	ns
			10		500	1000	
			15		375	750	
$t_{WH(d)}$	Clock Pulse Width		5	385	140		ns
			10	150	55		
			15	120	40		
f_{cl}	Clock Pulse Frequency		5		3.5	2	MHz
			10		9	5	
			15		12	6.5	
t_{TLH} t_{THL}	Clock Rise and Fall Time		5			15	μs
			10			15	
			15			15	
$t_{W(R)}$	Reset Pulse Width		5	1400	700		ns
			10	600	300		
			15	450	225		

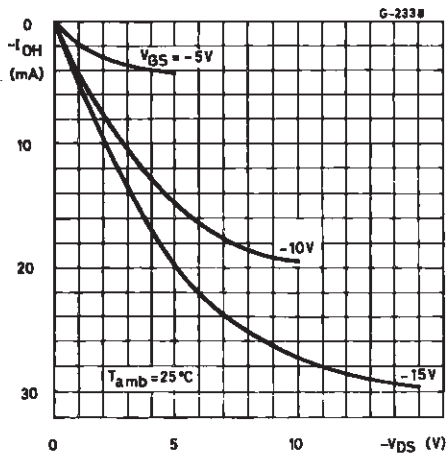
Typical Output Low (sink) Current Characteristics



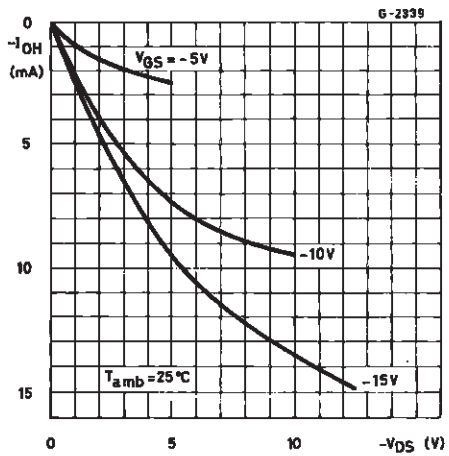
Minimum Output Low (sink) Current Characteristics



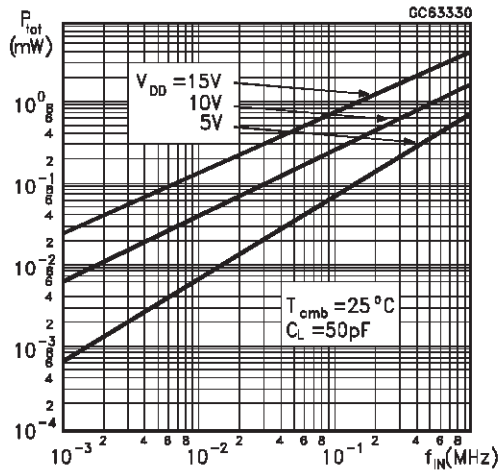
Typical Output High (source) Current Characteristics



Minimum Output High (source) Current Characteristics



Typical Power Dissipation vs, Frequency

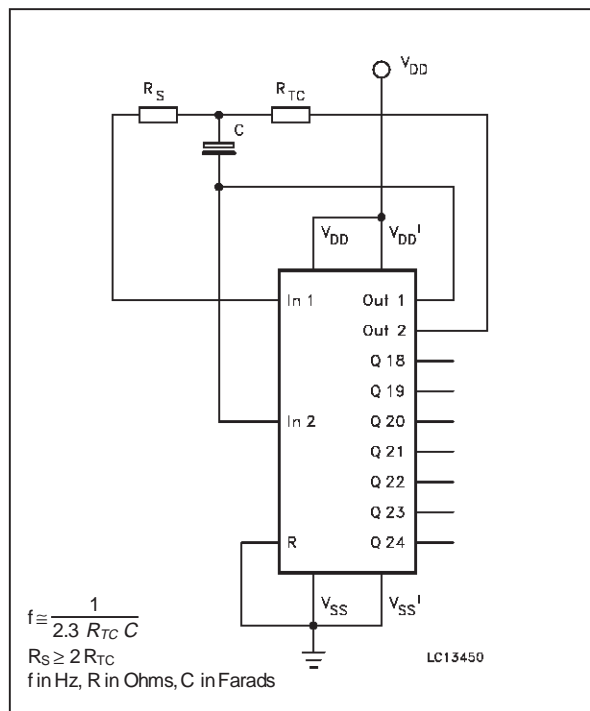


FUNCTIONAL TEST SEQUENCE

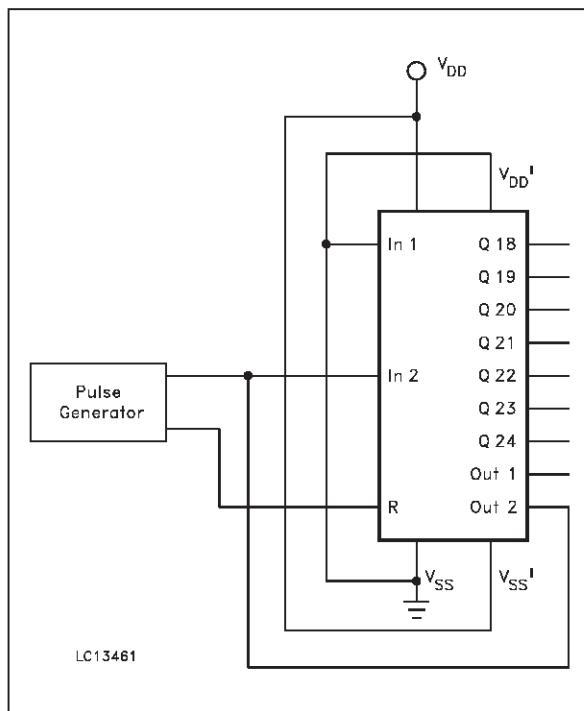
Inputs		Outputs				Comments
RESET	In2	Out2	V _{SS} '	V _{DD} '	Q18 thru Q24	
1	0	0	V _{DD}	GND	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In2 and Out2 are connected together
0	1	1	V _{DD}	GND	0	First "0" to "1" transition on In2, Out2 node.
0	0	0	V _{DD}	GND	0	255 "0" to "1" transitions are clocked into this In2, Out2 node.
0	1	1	V _{DD}	GND	0	
0	1	1	V _{DD}	GND	1	The 255th "0" to "1" transition.
0	0	0	V _{DD}	GND	1	
0	0	0	GND	GND	1	
0	1	0	GND	V _{DD}	1	Counter converted back to 24-stages in series mode.
0	1	0	GND	V _{DD}	1	Out2 converts back to an output
0	0	1	GND	V _{DD}	0	Counter ripples from an all "1" state to an all "0" stage.

A test function (see fig.8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flop are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In2) which will cause the counter to ripple from an all "1" state to an all "0" state.

RC Oscillator Circuit



Functional Test Circuit

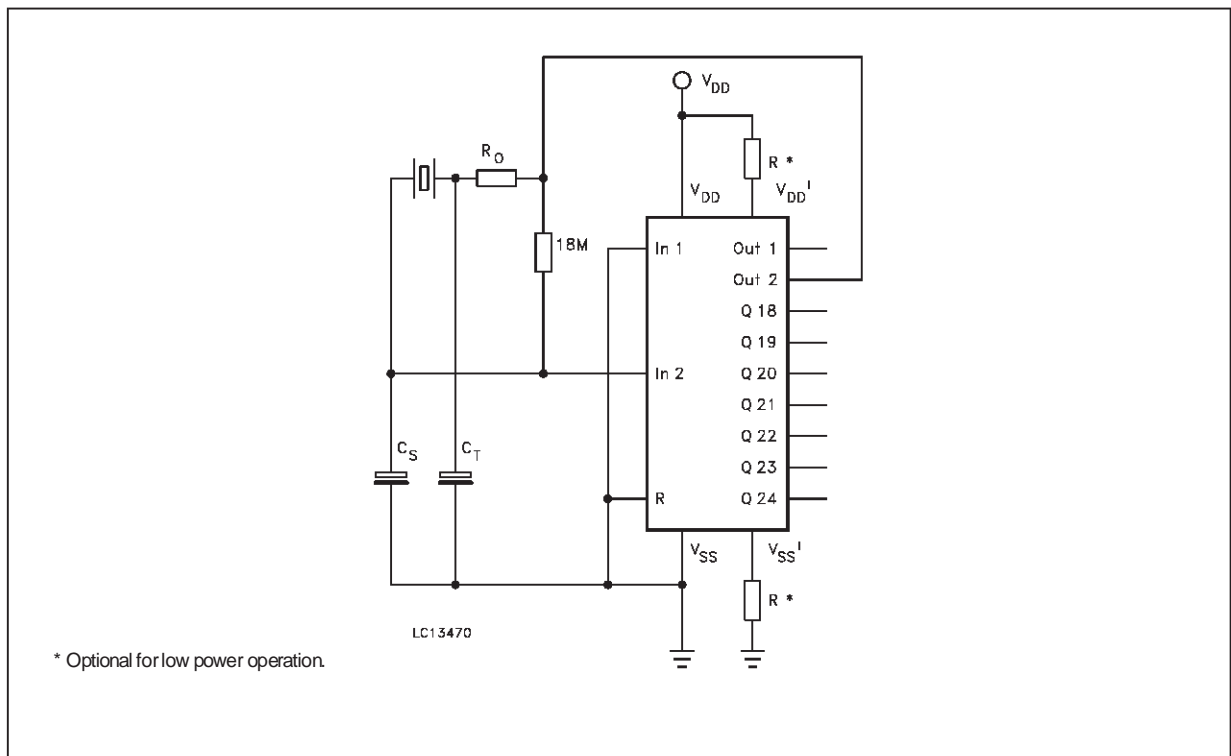


TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz CIRCUIT	50 kHz CIRCUIT	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1	6.2	$k\Omega$
External Resistor/Capacitor Values			
R_O	47	750	$k\Omega$
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} ($T_A = 25\text{ }^\circ\text{C}$)			
V_{DD} Change from 5V to 10V	6	2	ppm
V_{DD} Change from 10V to 15V	2	2	ppm
Frequency Change as a Function of Temperature ($V_{DD} = 10\text{ V}$)			
T_A Change from $-55\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$			
HCF4521B only	-4	-2	ppm
Complete Oscillator *	100	120	ppm
T_A Change from $25\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$			
HCF4521B only	-2	-2	ppm
Complete Oscillator *	-160	-560	ppm

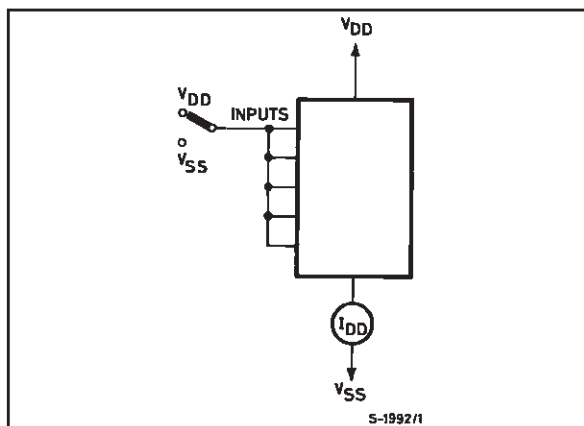
* Complete oscillator includes crystal, capacitors and resistors.

Crystal Oscillator Circuit

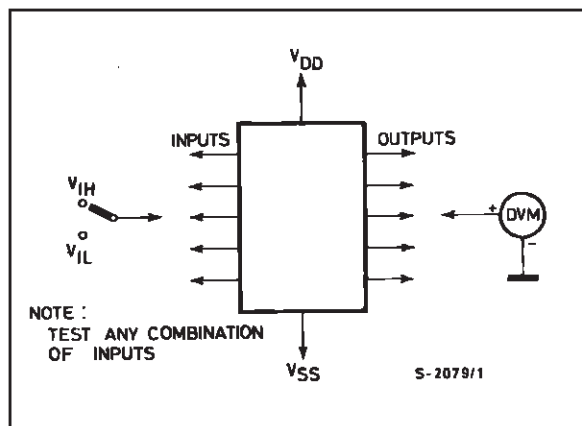


TEST CIRCUITS

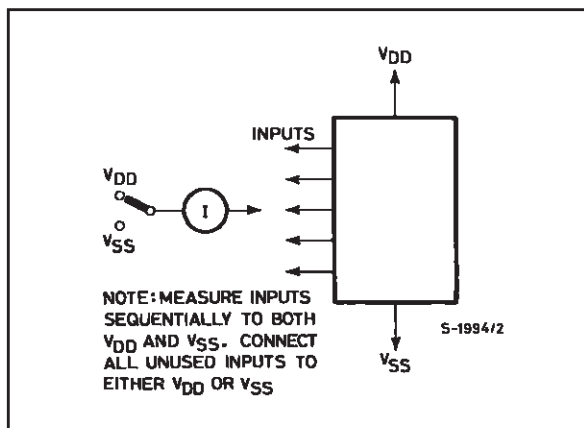
Quiescent Device Current.



Noise Immunity.

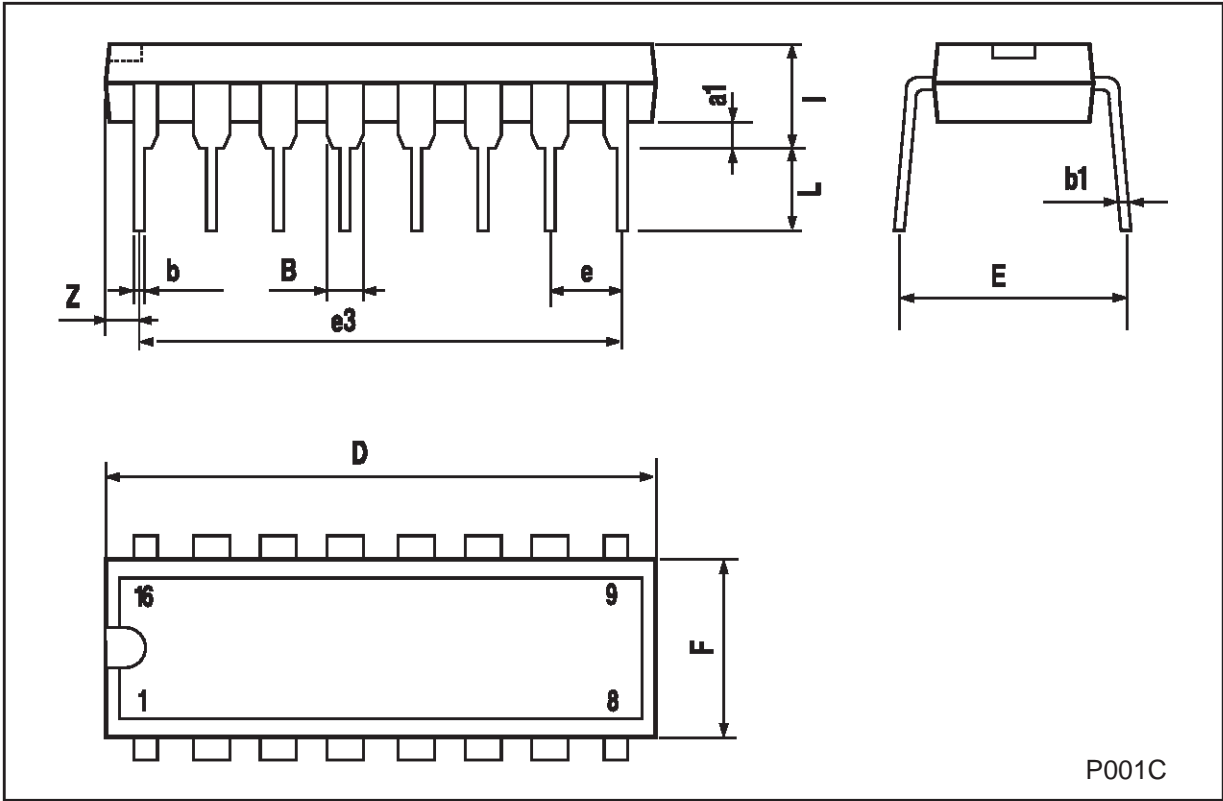


Input Leakage Current.



Plastic DIP-16 (0.25) MECHANICAL DATA

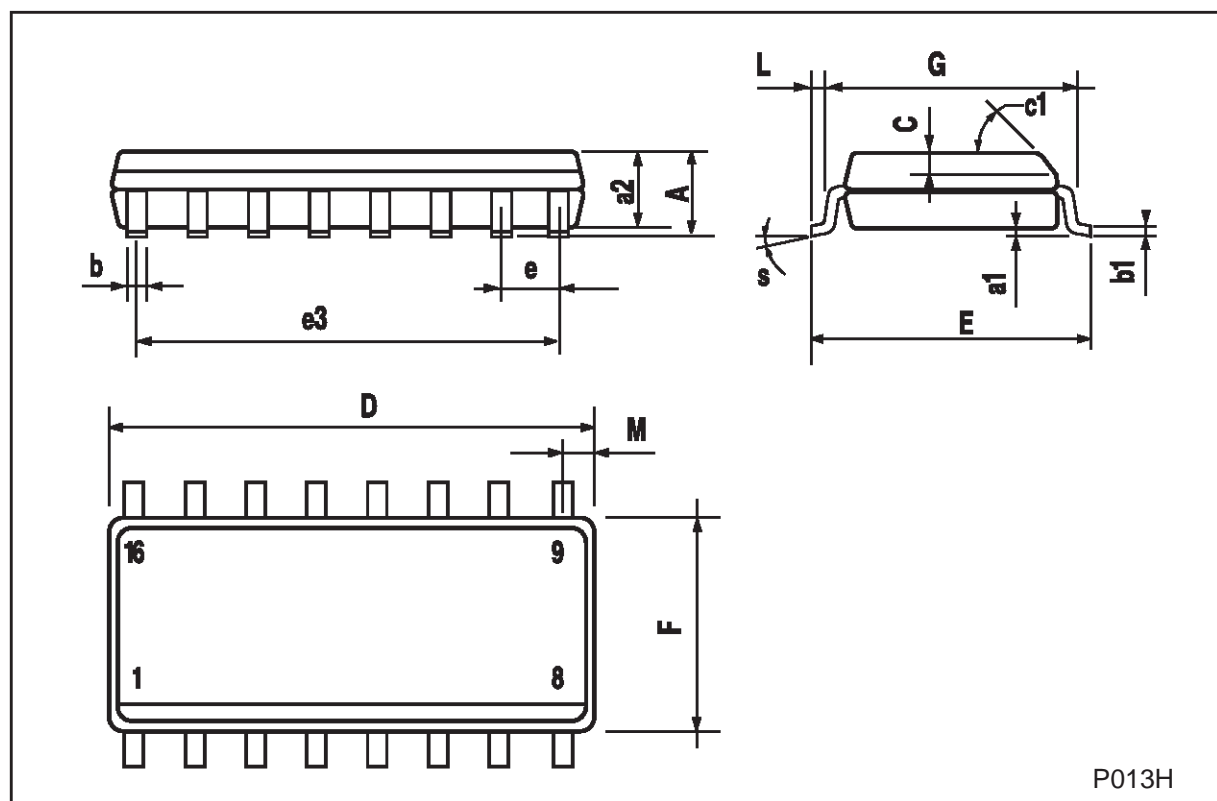
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



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