DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT162

Presettable synchronous BCD decade counter; synchronous reset

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Presettable synchronous BCD decade counter; synchronous reset

74HC/HCT162

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT162 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the “162” the clear function is synchronous.

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.
This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\ (CP\ to\ TC) + t_{SU}\ (CEP\ to\ CP)}$$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF; V_{CC} = 5 V	 19 21 11	 20 26 15	 ns ns ns
t_{PLH}	propagation delay CP to Q_n CP to TC CET to TC		 19 21 11	 20 19 10	 ns ns ns
f_{max}	maximum clock frequency		63	32	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	37	37	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$
   where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is
   V_I = GND to V_{CC}
   For HCT the condition is
   V_I = GND to V_{CC} − 1.5 V

Presettable synchronous BCD decade counter; synchronous reset

74HC/HCT162

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

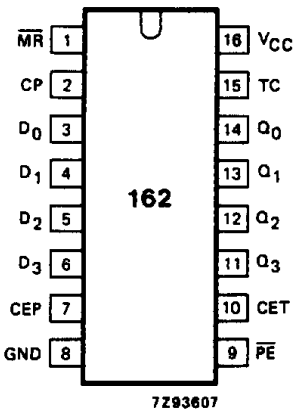


Fig.1 Pin configuration.

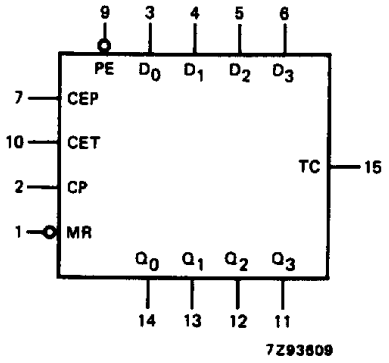


Fig.2 Logic symbol.

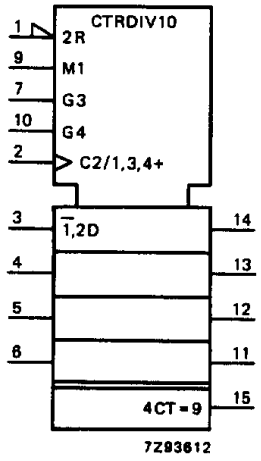


Fig.3 IEC logic symbol.

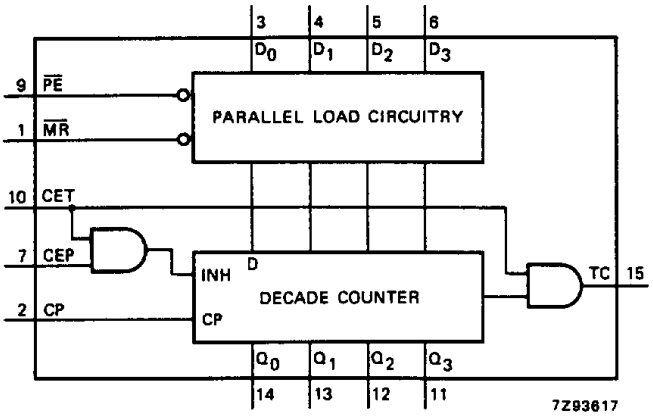


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (1)
count	h	↑	h	h	h	X	count	(1)
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(1) L

Notes

1. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).
   H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

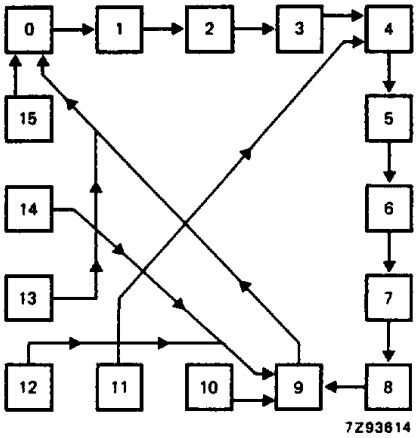


Fig.5 State diagram.

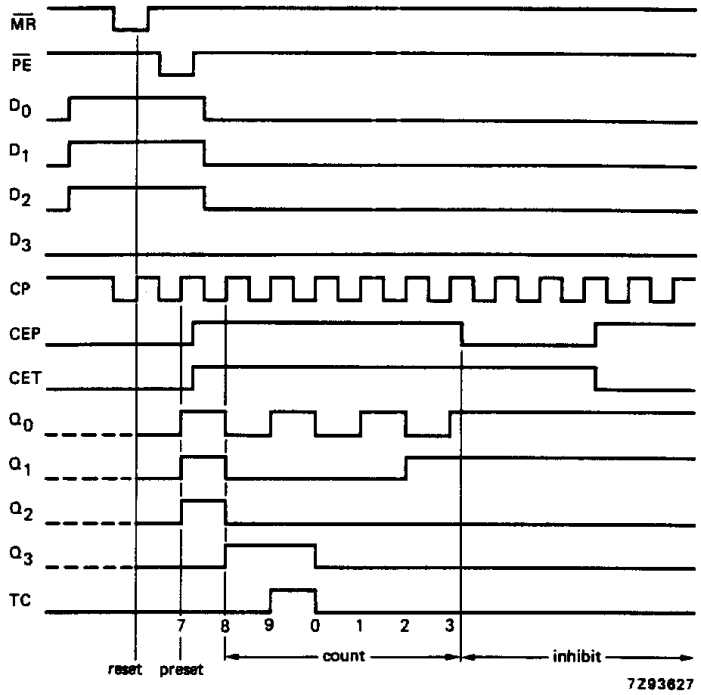


Fig.6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

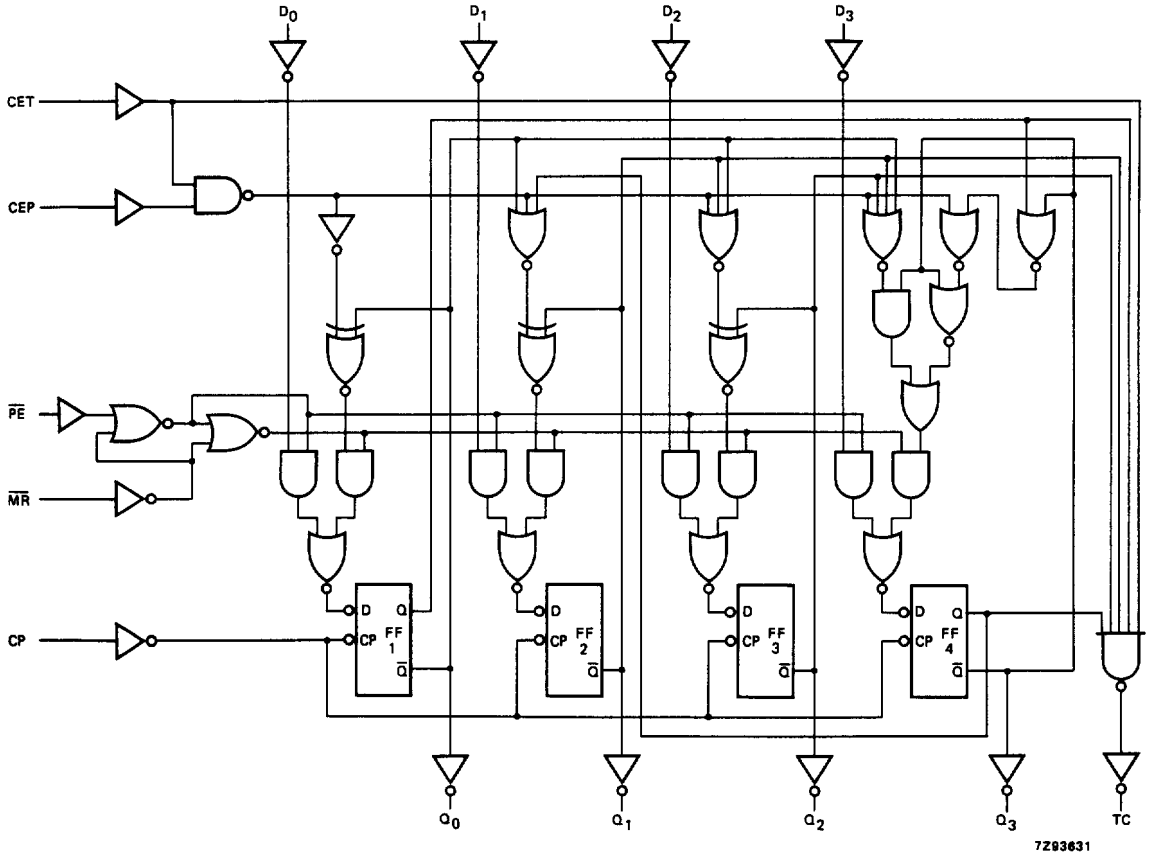


Fig.7 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		58 21 17	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay CET to TC		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time $\overline{MR}$, D_n to CP	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 9 and 11
t_{su}	set-up time $\overline{PE}$ to CP	135 27 23	39 14 11		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time CEP, CET to CP	200 40 34	69 25 20		250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig.12
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0 0 0	–17 –6 –5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 9, 11 and 12
f_{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	0.80
CEP	0.25
D_n	0.25
CET	1.50
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		24	43		54		65	ns	4.5	Fig.8
t_{PHL}	propagation delay CP to TC		30	51		64		77	ns	4.5	Fig.8
t_{PLH}	propagation delay CP to TC		22	45		56		68	ns	4.5	Fig.8
t_{PHL}	propagation delay CET to TC		18	35		44		53	ns	4.5	Fig.9
t_{PLH}	propagation delay CET to TC		12	24		30		36	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.8
t_{su}	set-up time D_n to CP	20	9		25		30		ns	4.5	Fig.9
t_{su}	set-up time $\overline{PE}$ to CP	35	16		44		53		ns	4.5	Fig.9
t_{su}	set-up time CEP, CET to CP	40	23		50		60		ns	4.5	Fig.12
t_{su}	set-up time $\overline{MR}$ to CP	20	12		25		30		ns	4.5	Fig.11
t_h	hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	0	−10		0		0		ns	4.5	Figs 9, 11 and 12
f_{max}	maximum clock pulse frequency	17	29		14		11		MHz	4.5	Fig.8

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

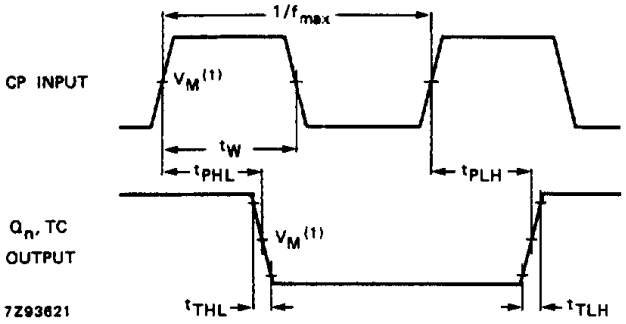


Fig.8 Waveforms showing the clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

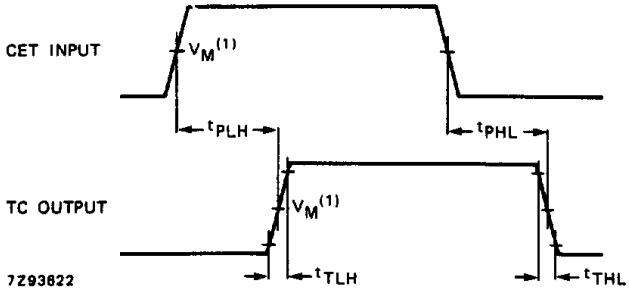


Fig.9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

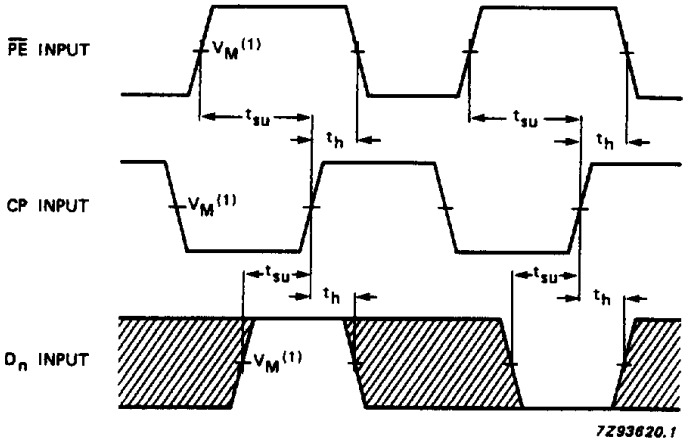
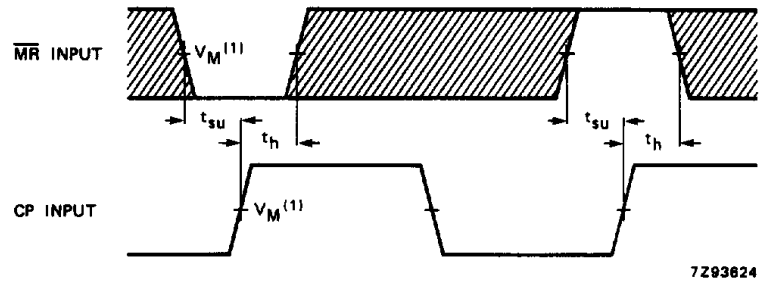


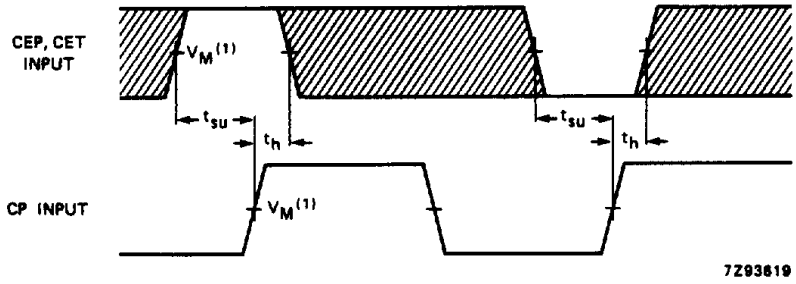
Fig.10 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing the $\overline{MR}$ set-up and hold times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.12 Waveforms showing the CEP and CET set-up and hold times.

APPLICATION INFORMATION

The HC/HCT162 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.

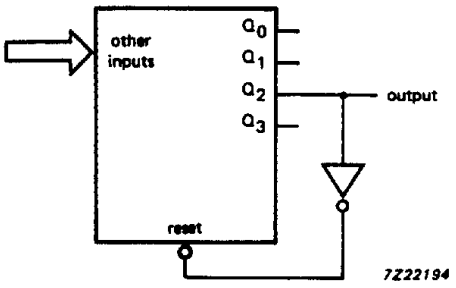


Fig.13 Modulo-5 counter.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.