

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT283**

**4-bit binary full adder with fast carry**

Product specification  
File under Integrated Circuits, IC06

December 1990

# 4-bit binary full adder with fast carry

# 74HC/HCT283

## FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A<sub>n</sub> plus B<sub>n</sub>) plus the incoming carry. The binary sum appears on the sum outputs (Σ<sub>1</sub> to Σ<sub>4</sub>) and the out-going carry (C<sub>OUT</sub>) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the “283” can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ<sub>1</sub> to Σ<sub>4</sub> and C<sub>OUT</sub> should be interpreted also as active LOW. With active HIGH inputs, C<sub>IN</sub> must be held LOW when no “carry in” is intended. Interchanging inputs of equal weight does not affect the operation, thus C<sub>IN</sub>, A<sub>1</sub>, B<sub>1</sub> can be assigned arbitrarily to pins 5, 6, 7, etc.

See the “583” for the BCD version.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	C <sub>IN</sub> to Σ <sub>1</sub>		16	15	ns
	C <sub>IN</sub> to Σ <sub>2</sub>		18	21	ns
	C <sub>IN</sub> to Σ <sub>3</sub>		20	23	ns
	C <sub>IN</sub> to Σ <sub>4</sub>		23	27	ns
	A <sub>n</sub> or B <sub>n</sub> to Σ <sub>n</sub>		21	25	ns
	C <sub>IN</sub> to C <sub>OUT</sub>		20	23	ns
A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>	20	24	ns		
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	88	92	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

# 4-bit binary full adder with fast carry

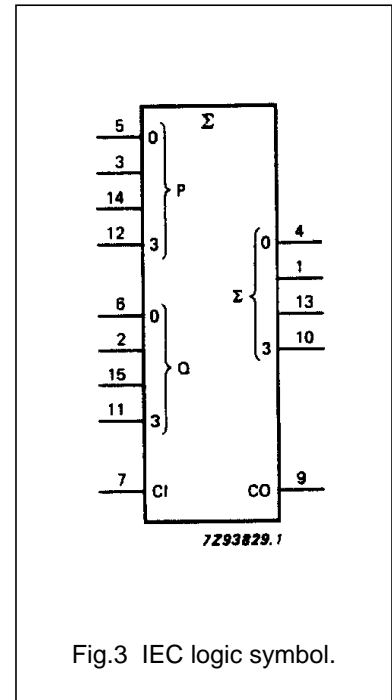
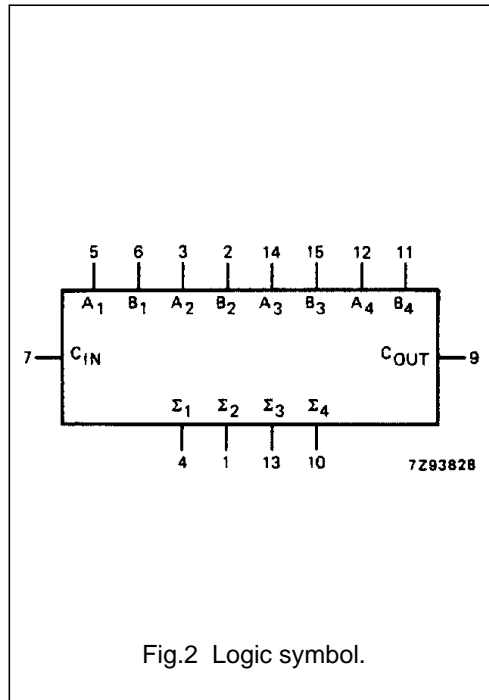
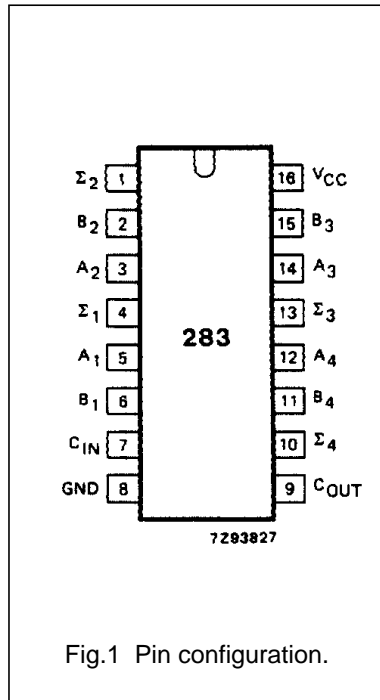
# 74HC/HCT283

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	$\Sigma_1$ to $\Sigma_4$	sum outputs
5, 3, 14, 12	$A_1$ to $A_4$	A operand inputs
6, 2, 15, 11	$B_1$ to $B_4$	B operand inputs
7	$C_{IN}$	carry input
8	GND	ground (0 V)
9	$C_{OUT}$	carry output
16	$V_{CC}$	positive supply voltage



4-bit binary full adder with fast carry

74HC/HCT283

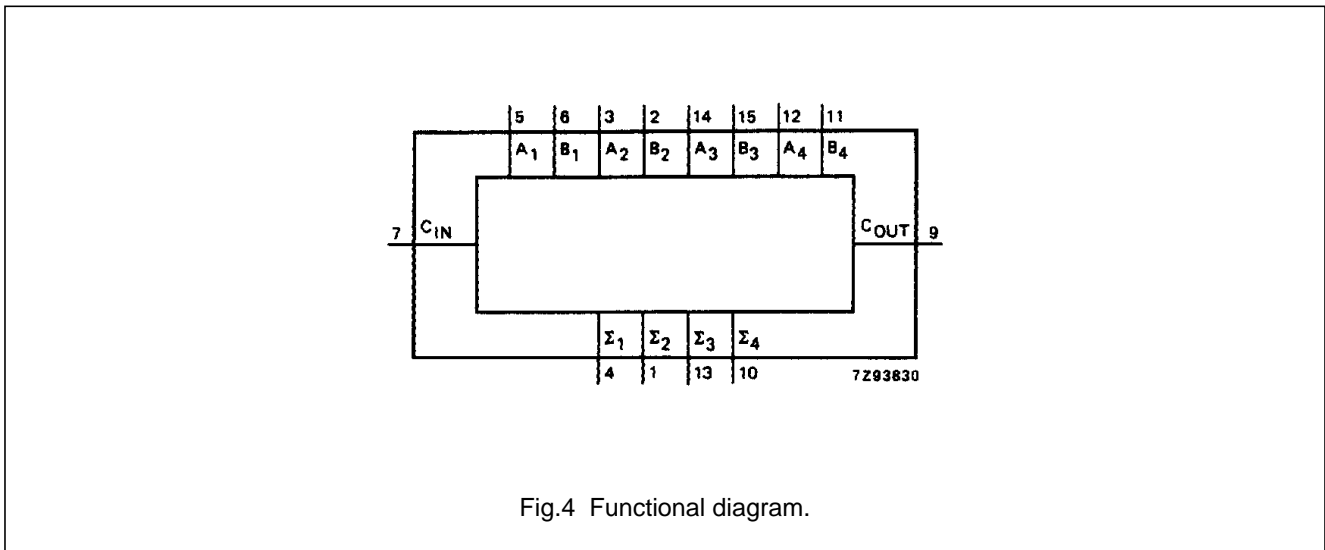


Fig.4 Functional diagram.

FUNCTION TABLE

PINS	C <sub>IN</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	Σ <sub>1</sub>	Σ <sub>2</sub>	Σ <sub>3</sub>	Σ <sub>4</sub>	C <sub>OUT</sub>	EXAMPLE <sup>(2)</sup>
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(3)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(4)

Note

1. H = HIGH voltage level  
L = LOW voltage level
2. **example**  
 1001  
 1010  
 -----  
 10011
3. for active HIGH, example = (9 + 10 = 19)
4. for active LOW, example = (carry + 6 + 5 = 12)

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74HC/HCT283

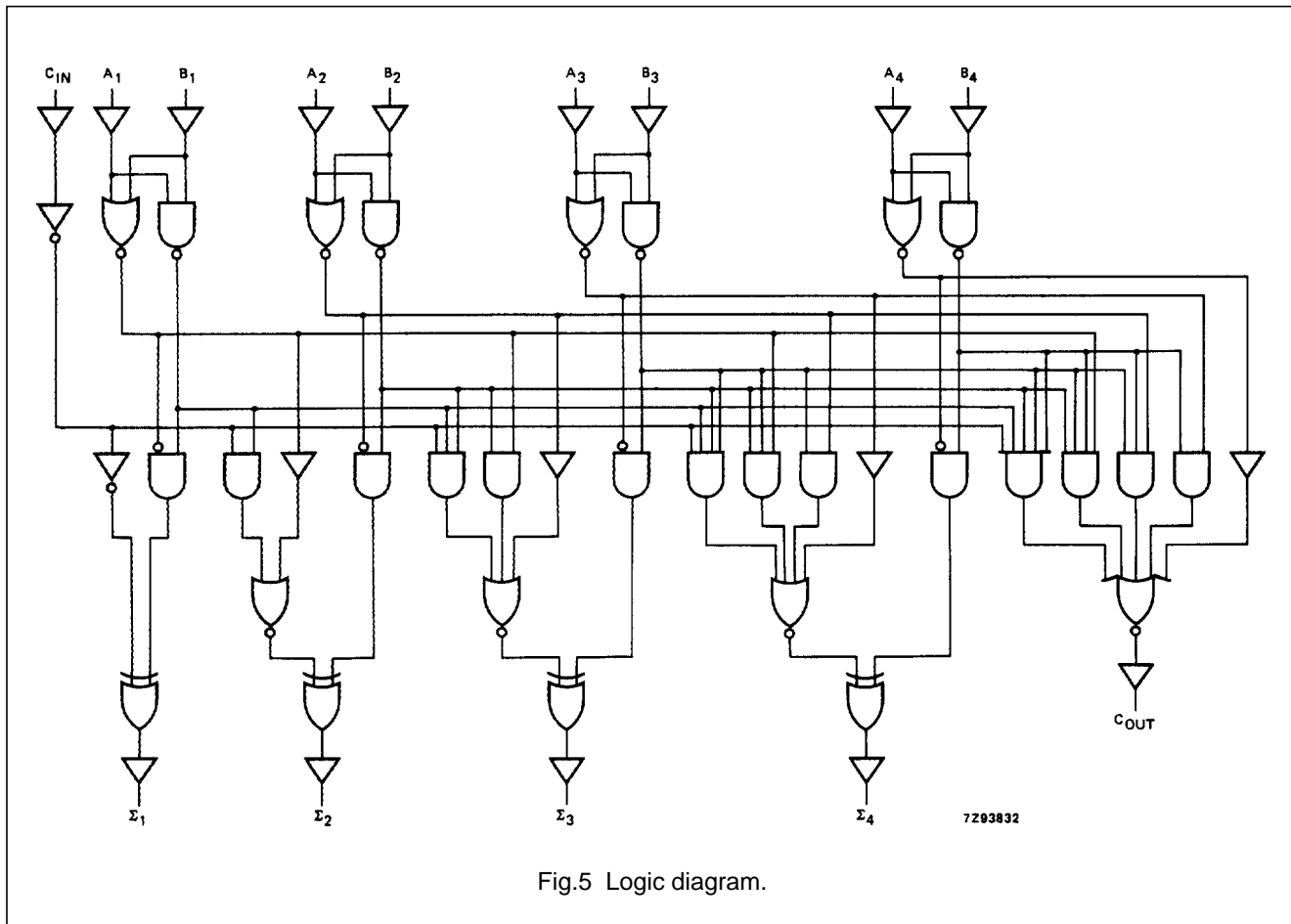


Fig.5 Logic diagram.

## 4-bit binary full adder with fast carry

## 74HC/HCT283

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>1</sub>		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>2</sub>		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>3</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>4</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to Σ <sub>n</sub>		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to C <sub>OUT</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

## 4-bit binary full adder with fast carry

## 74HC/HCT283

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C <sub>IN</sub>	1.50
B <sub>2</sub> , A <sub>2</sub> , A <sub>1</sub>	1.00
B <sub>1</sub>	0.40
B <sub>4</sub> , A <sub>4</sub> , A <sub>3</sub> , B <sub>3</sub>	0.50

**AC CHARACTERISTICS FOR 74HCT**

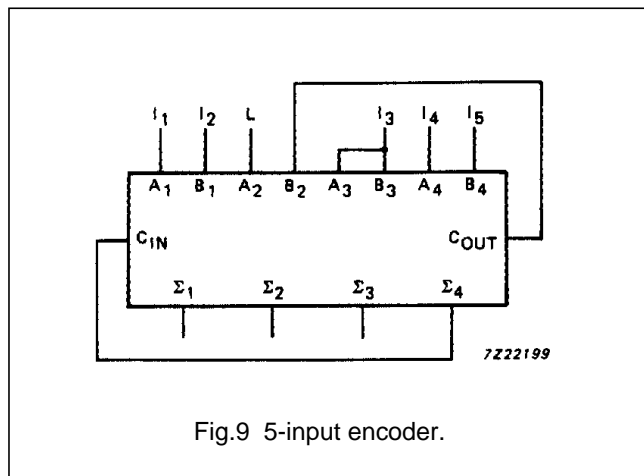
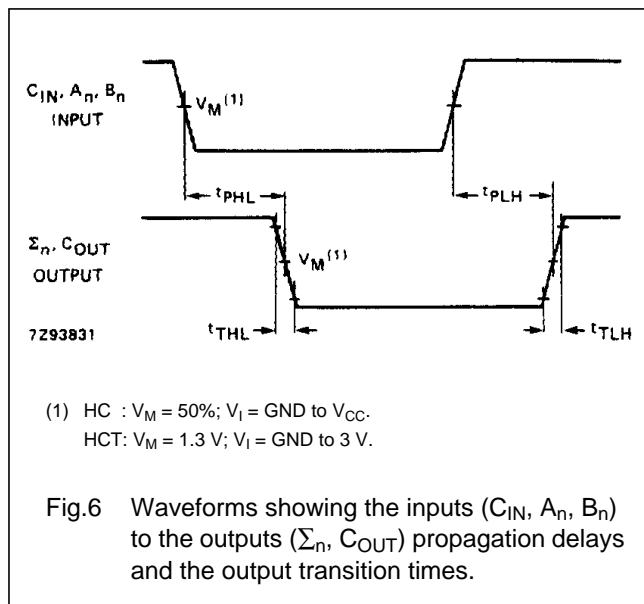
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_1$		18	31		39		47	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_2$		25	43		54		65	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_3$		27	46		58		69	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_4$		31	53		66		80	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to $\Sigma_n$		29	49		61		74	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to C <sub>OUT</sub>		27	46		58		69	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>		28	48		60		72	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6	

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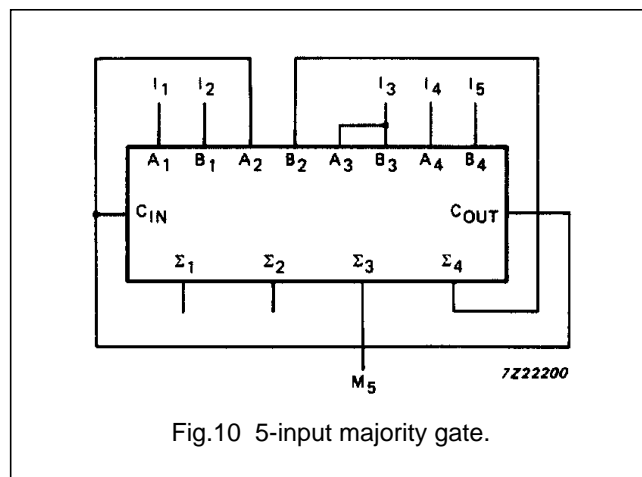
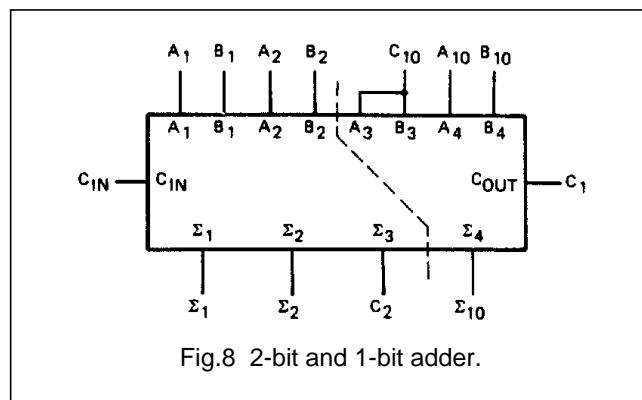
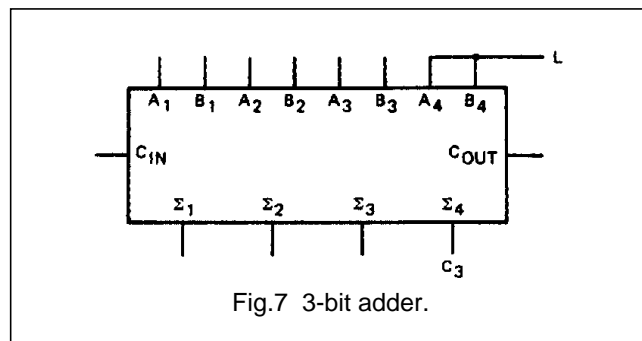
## AC WAVEFORMS



### Notes to Figs 7 to 10

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $\Sigma_3$  dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $\Sigma_2$ ) is used simply as means of transferring the carry into the fourth stage (via  $A_2$  and  $B_2$ ) and transferring the carry from the second stage on  $\Sigma_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, HIGH or LOW, they do not influence  $\Sigma_2$ . Similarly, when  $A_2$  and  $B_2$  are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the

## APPLICATION INFORMATION



inputs are equally weighted. The outputs  $\Sigma_0$ ,  $\Sigma_1$  and  $\Sigma_2$  produce a binary number equal to the number inputs ( $I_1$  to  $I_5$ ) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs ( $I_1$  to  $I_5$ ) are HIGH, the output  $M_5$  is HIGH.

### PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".