

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT299**

**8-bit universal shift register; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit universal shift register; 3-state

## 74HC/HCT299

## FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
  - shift left
  - shift right
  - hold (store)
  - load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os), standard (serial outputs)
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S<sub>0</sub> and S<sub>1</sub>), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O<sub>0</sub> to I/O<sub>7</sub>) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q<sub>0</sub> and Q<sub>7</sub>) are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input ( $\overline{\text{MR}}$ ) overrides the S<sub>n</sub> and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ( $\overline{\text{OE}}_1$  or  $\overline{\text{OE}}_2$ ) disables the 3-state buffers and the I/O<sub>n</sub> outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub>, when in preparation for a parallel load operation.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> , Q <sub>7</sub> CP to I/O <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	20	19	ns
t <sub>PHL</sub>	$\overline{\text{MR}}$ to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		20	19	ns
f <sub>max</sub>	maximum clock frequency		20	23	ns
C <sub>I</sub>	input capacitance		50	46	MHz
C <sub>I/O</sub>	input/output capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	10	10	pF
			120	125	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

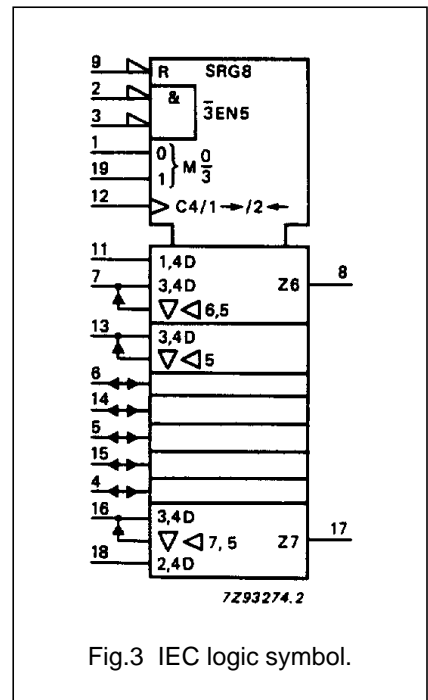
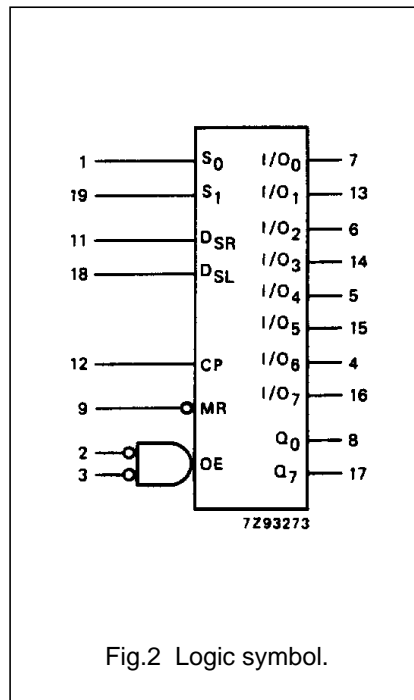
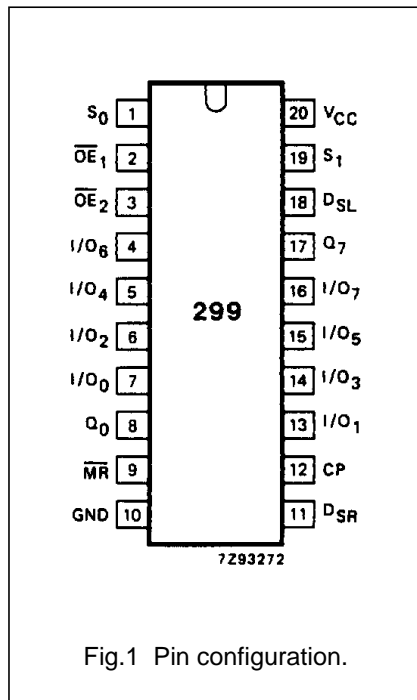
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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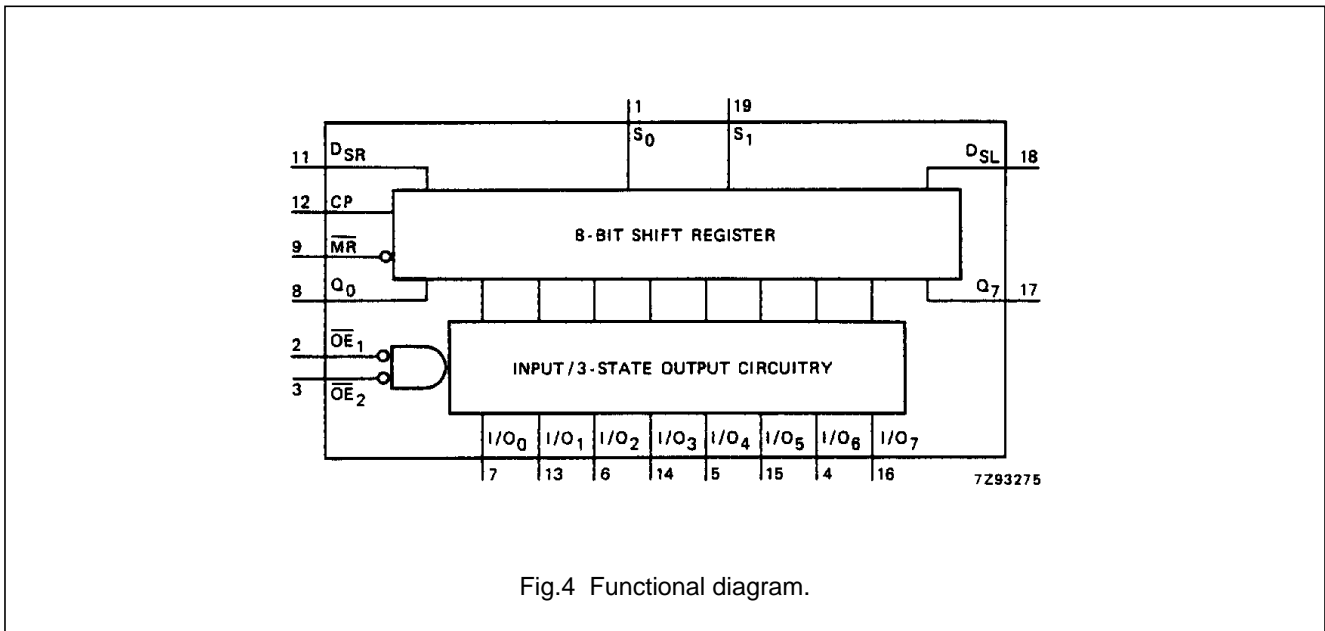
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$S_0, S_1$	mode select inputs
2, 3	$\overline{OE}_1, \overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O <sub>0</sub> to I/O <sub>7</sub>	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q <sub>0</sub> , Q <sub>7</sub>	serial outputs (standard output)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D <sub>SR</sub>	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D <sub>SL</sub>	serial data shift-left input
20	V <sub>CC</sub>	positive supply voltage



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**MODE SELECT TABLE**

INPUTS				RESPONSE
MR	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	asynchronous reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↑	parallel load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↑	shift right; D <sub>SR</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> etc.
H	H	L	↑	shift left; D <sub>SL</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> etc.
H	L	L	X	hold

**Notes**

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition

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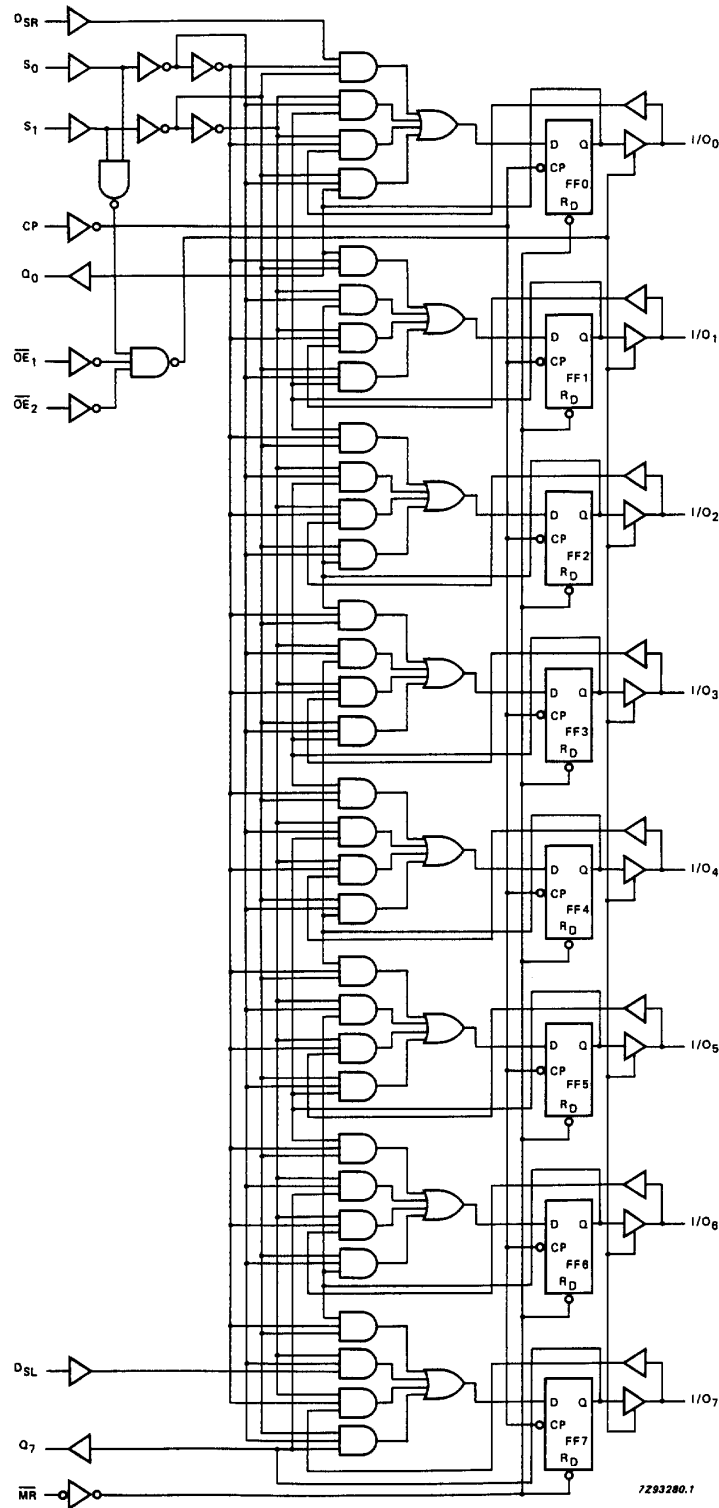


Fig.5 Logic diagram.

## 8-bit universal shift register; 3-state

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)  
standard (serial outputs)

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> , Q <sub>7</sub>		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to I/O <sub>n</sub>		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> /	propagation delay MR to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.7
t <sub>PZH</sub>	3-state output enable time $\overline{OE}_n$ to I/O <sub>n</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t <sub>PZL</sub>	3-state output enable time $\overline{OE}_n$ to I/O <sub>n</sub>		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.9
t <sub>PHZ</sub>	3-state output disable time $\overline{OE}_n$ to I/O <sub>n</sub>		66 24 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.9
t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_n$ to I/O <sub>n</sub>		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver (I/O <sub>n</sub> )		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard (Q <sub>0</sub> , Q <sub>7</sub> )		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>rem</sub>	removal time MR to CP	5	-14		5		5		ns	2.0	Fig.7
		5	-5		5		5			4.5	
		5	-4		5		5			6.0	
t <sub>su</sub>	set-up time D <sub>SR</sub> , D <sub>SL</sub> to CP	100	33		125		150		ns	2.0	Fig.6
		20	12		25		30			4.5	
		17	10		21		26			6.0	
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	100	33		125		150		ns	2.0	Fig.8
		20	12		25		30			4.5	
		17	10		21		26			6.0	
t <sub>su</sub>	set-up time I/O <sub>n</sub> to CP	125	39		155		190		ns	2.0	Fig.6
		25	14		31		38			4.5	
		21	11		26		32			6.0	
t <sub>h</sub>	hold time I/O <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	0	-14		0		0		ns	2.0	Fig.6
		0	-5		0		0			4.5	
		0	-4		0		0			6.0	
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	0	-28		0		0		ns	2.0	Fig.8
		0	-10		0		0			4.5	
		0	-8		0		0			6.0	
f <sub>max</sub>	maximum clock pulse frequency	5.0	15		4.0		3.4		MHz	2.0	Fig.6
		25	45		20		17			4.5	
		29	54		24		20			6.0	

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)  
standard (serial outputs)

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I/O <sub>n</sub>	0.25
D <sub>SR</sub> , D <sub>SL</sub>	0.25
CP, S <sub>0</sub>	0.60
$\overline{MR}$ , S <sub>1</sub>	0.25
$\overline{OE}_n$	0.30



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## AC CHARACTERISTICS FOR 74HCT

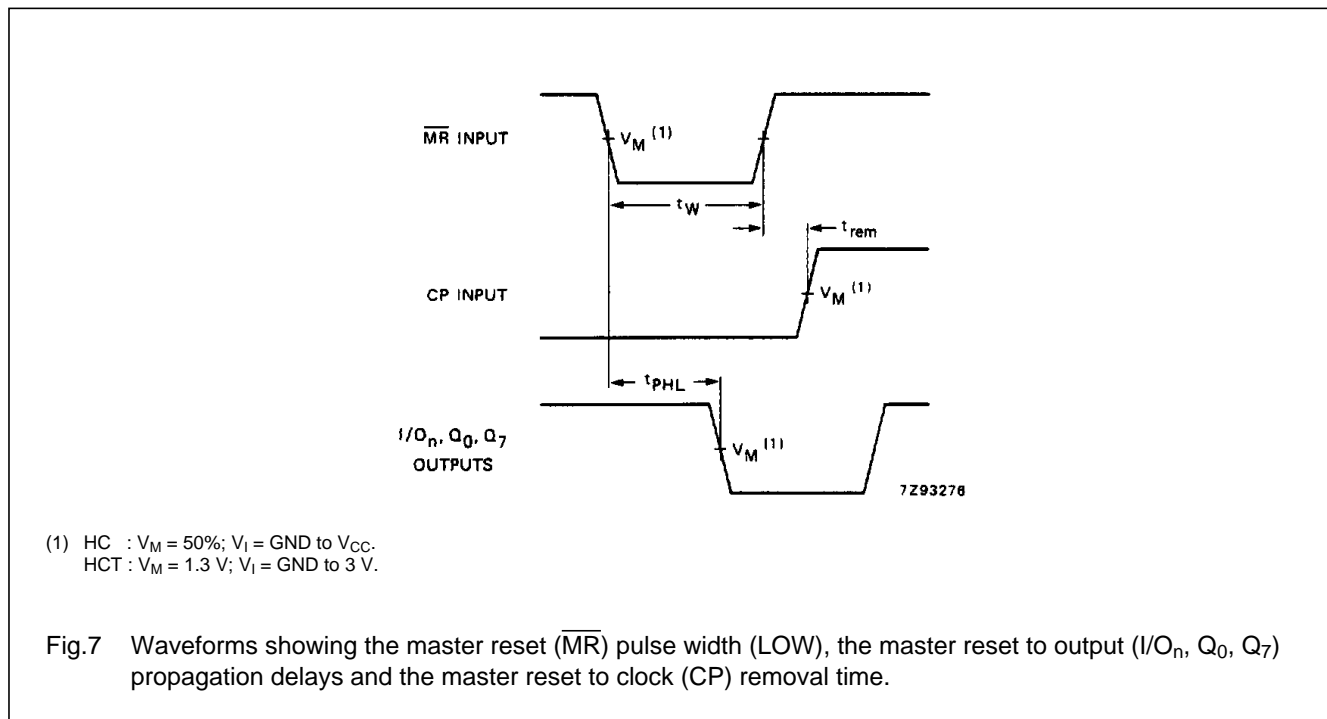
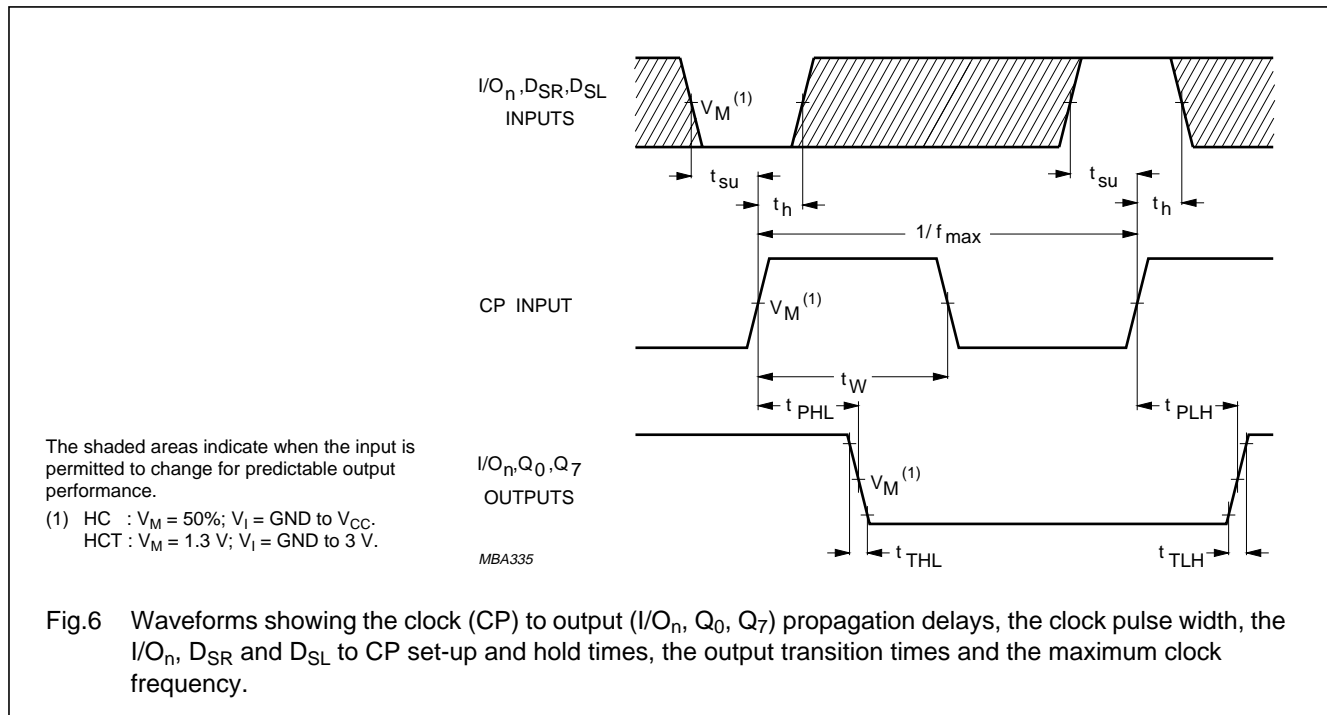
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> , Q <sub>7</sub>		22	37		46		56	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to I/O <sub>n</sub>		22	37		46		56	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay $\overline{MR}$ to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		27	46		58		69	ns	4.5	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_n$ to I/O <sub>n</sub>		19	30		38		45	ns	4.5	Fig.9
t <sub>PHZ</sub>	3-state output disable time $\overline{OE}_n$ to I/O <sub>n</sub>		24	37		46		56	ns	4.5	Fig.9
t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_n$ to I/O <sub>n</sub>		20	32		40		48	ns	4.5	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver (I/O <sub>n</sub> )		5	12		15		18	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard (Q <sub>0</sub> , Q <sub>7</sub> )		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig.6
t <sub>W</sub>	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig.7
t <sub>rem</sub>	removal time MR to CP	10	2		9		11		ns	4.5	Fig.7
t <sub>su</sub>	set-up time I/O <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	25	14		31		38		ns	4.5	Fig.6
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	32	18		40		48		ns	4.5	Fig.8
t <sub>h</sub>	hold time I/O <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	0	-11		0		0		ns	4.5	Fig.6
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	0	-17		0		0		ns	4.5	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	25	42		20		17		MHz	4.5	Fig.6

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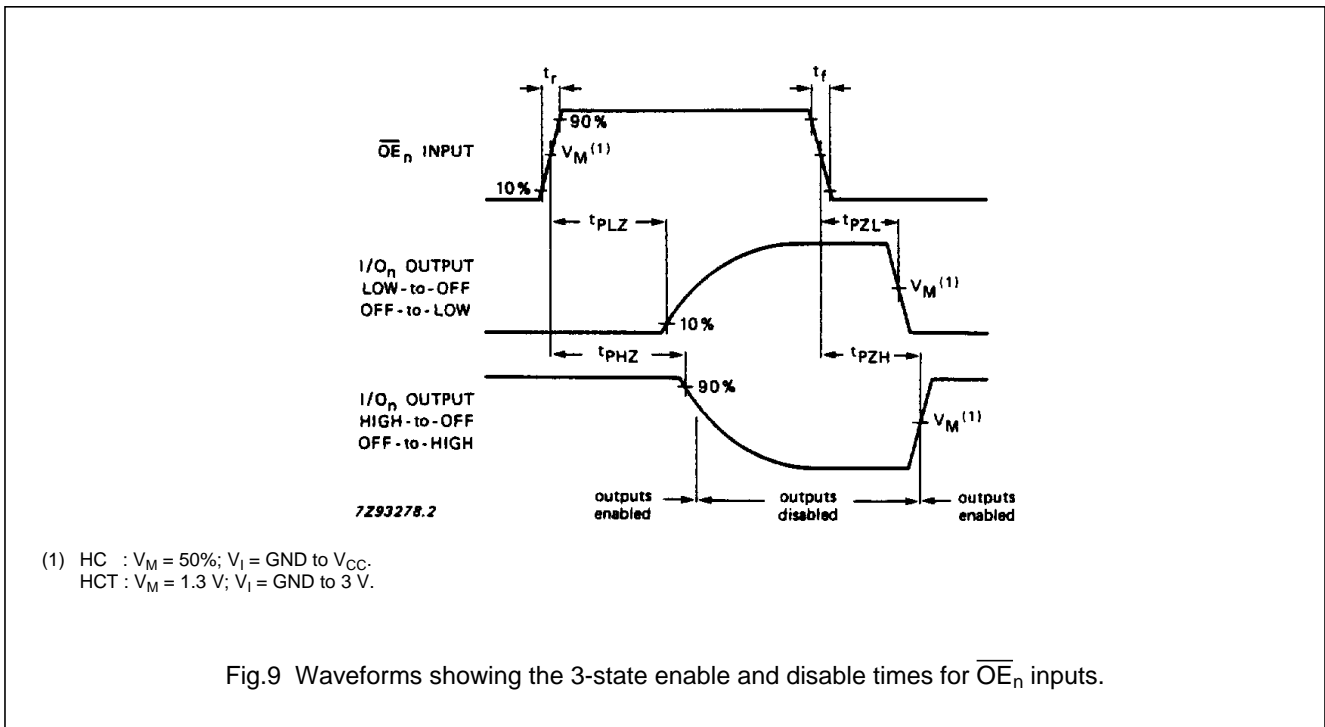
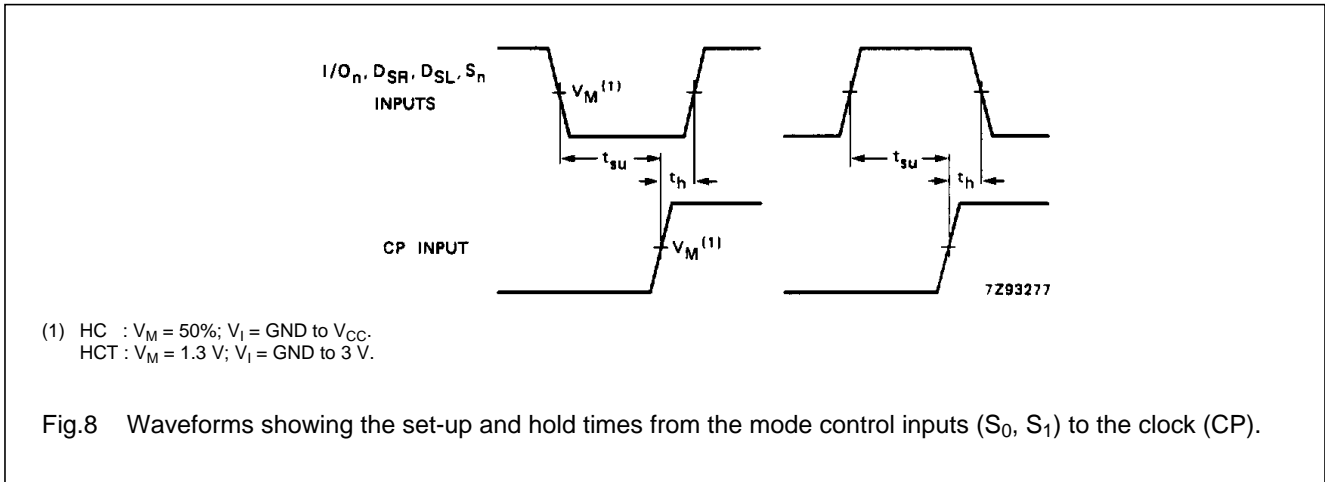
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AC WAVEFORMS



8-bit universal shift register; 3-state

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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".