

**8 BIT ADDRESSABLE LATCH**

- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTER
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MAXIMUM INPUT CURRENT OF 1 $\mu$ A AT 18V (full package-temperature range), 100nA AT 18V AND 25 $^{\circ}$ C
- NOISE MARGIN (full package-temperature range) = 1V AT V<sub>DD</sub> = 5V, 2V AT V<sub>DD</sub> = 10V, 2.5V AT V<sub>DD</sub> = 15V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF 'B' SERIES CMOS DEVICES"

**APPLICATION**

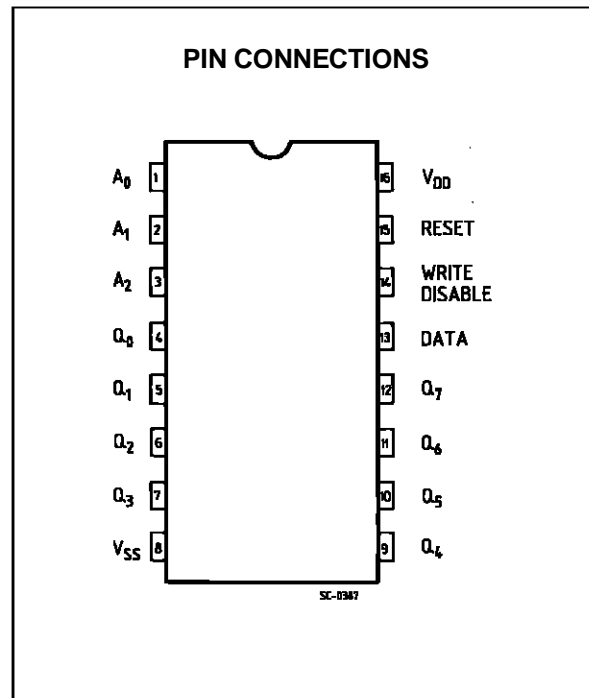
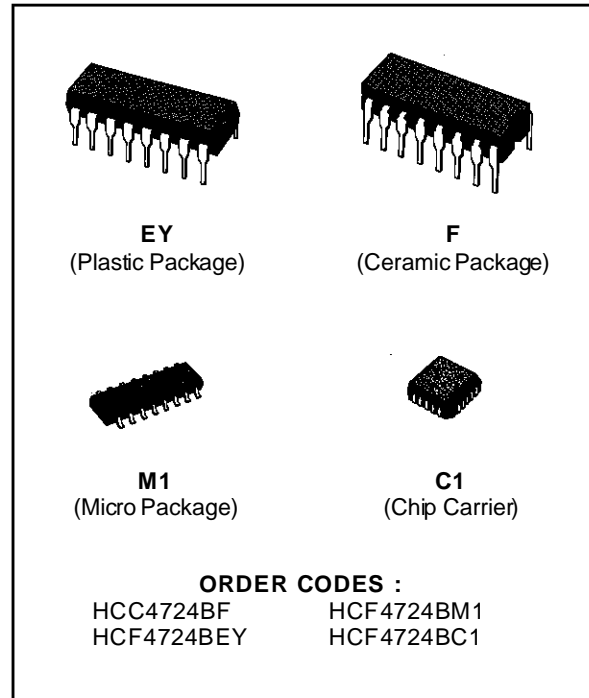
- MULTI-LINE DECODERS
- A/D CONVERTERS

**DESCRIPTION**

The **HCC/HCF4724B** 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

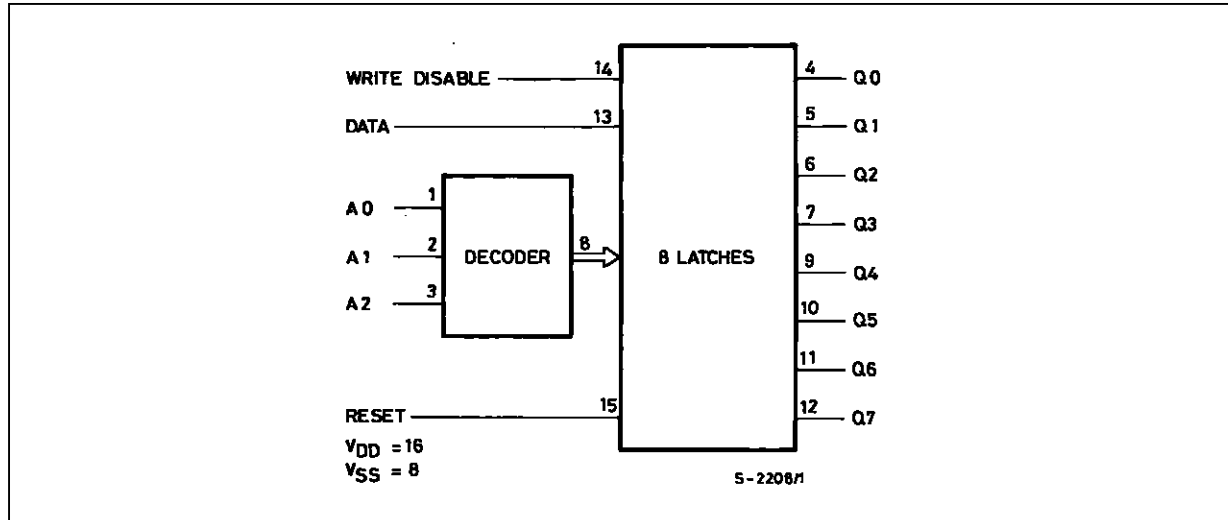
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>) and when WRITE DISABLE is at low level. When WRITE DISABLE is high, data entry is inhibited however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer ; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.



# HCC/HCF4724B

## FUNCTIONAL DIAGRAM



## ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
$V_{DD}^*$	Supply Voltage: <b>HCC</b> Types <b>HCF</b> Types	-0.5 to +20 -0.5 to +18	V V
$V_i$	Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_i$	DC Input Current (any one input)	$\pm 10$	mA
$P_{tot}$	Total Power Dissipation (per package) Dissipation per Output Transistor for $T_{op} =$ Full Package Temperature Range	200 100	mW mW
$T_{op}$	Operating Temperature: <b>HCC</b> Types <b>HCF</b> Types	-55 to +125 -40 to +85	$^{\circ}C$ $^{\circ}C$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

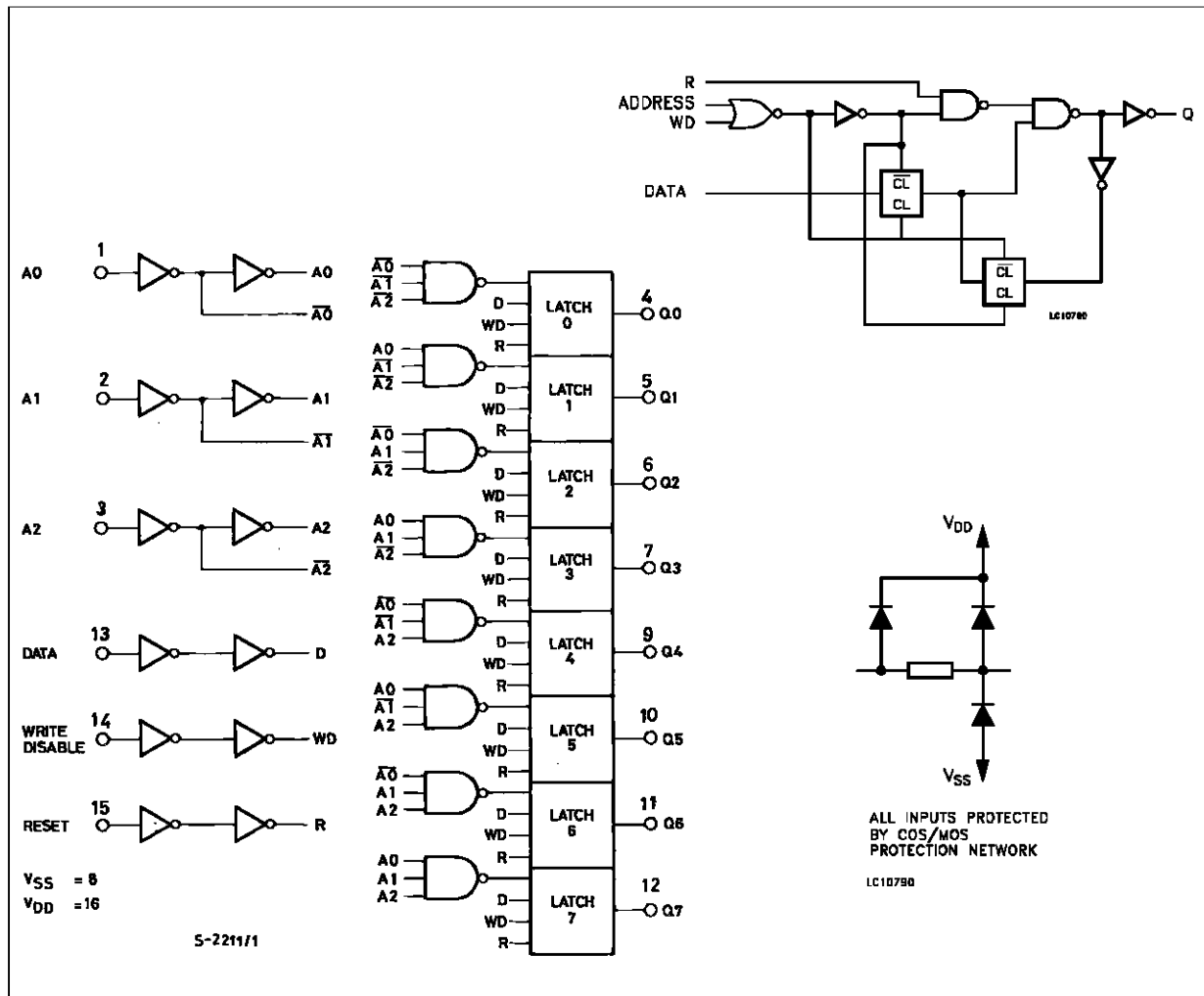
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

\* All voltage values are referred to  $V_{SS}$  pin voltage.

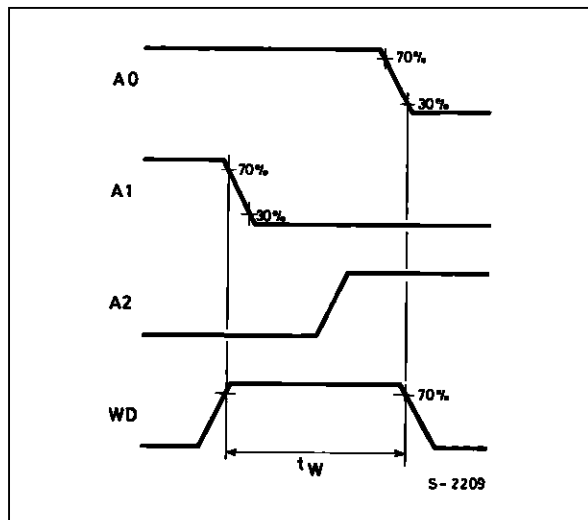
## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage: <b>HCC</b> Types <b>HCF</b> Types	3 to 18 3 to 15	V V
$V_i$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature: <b>HCC</b> Types <b>HCF</b> Types	-55 to +125 -40 to +85	$^{\circ}C$ $^{\circ}C$

LOGIC DIAGRAM



Definition of WRITE DISABLE ON Time



MODE SELECTION

TYPE	WD	R	Addressed Latch	Unaddressed Latch
A	0	0	Follows Data	Hold Previous State
B	0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
C	1	0	Hold Previous State	
D	1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R= RESET

# HCC/HCF4724B

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>LOW</sub> *		25 °C			T <sub>HIGH</sub> *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	HCC Types	0/5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000		
		HCF Types	0/5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
0/15				15		80		0.04	80		600			
V <sub>OH</sub>	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V <sub>OL</sub>	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V <sub>IH</sub>	Input High Voltage	0.5/4.5		< 1	5	3.5		3.5			3.5		V	
		1/9		< 1	10	7		7			7			
		1.5/13.5		< 1	15	11		11			11			
V <sub>IL</sub>	Input Low Voltage	4.5/0.5		< 1	5		1.5			1.5		1.5	V	
		9/1		< 1	10		3			3		3		
		13.5/1.5		< 1	15		4			4		4		
I <sub>OH</sub>	Output Drive Current	HCC Types	0/5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4			
		HCF Types	0/5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/5	4.6		5	-0.61		-0.51	-1		-0.42		
0/10	9.5			10	-1.5		-1.3	-2.6		-1.1				
0/15	13.5		15	-4		-3.4	-6.8		-2.8					
I <sub>OL</sub>	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I <sub>IH</sub> , I <sub>IL</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 0.1$		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$	$\mu$ A	
C <sub>I</sub>	Input Capacitance		Any Input						5	7.5			pF	

\* T<sub>LOW</sub> = -55 °C for HCC device; -40 °C for HCF device.

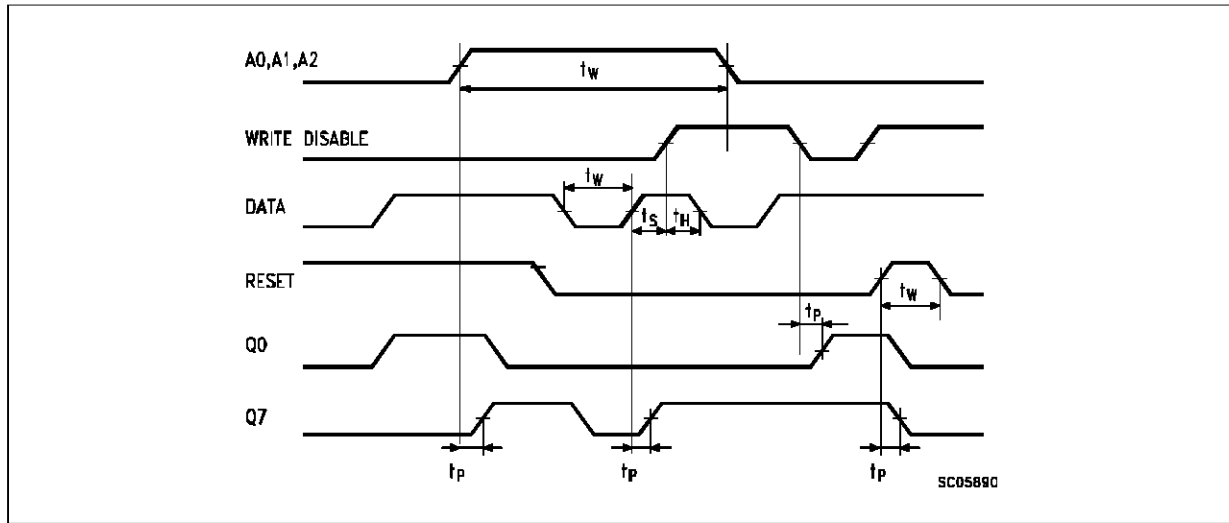
\* T<sub>HIGH</sub> = +125 °C for HCC device; +85 °C for HCF device.

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub> = 5V, 2V min. with V<sub>DD</sub> = 10V, 2.5V min. with V<sub>DD</sub> = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ K}\Omega$ , typical temperature coefficient for all  $V_{DD}$  values is  $03\text{ } \%/^{\circ}\text{C}$ , all input rise and fall times =  $20\text{ ns}$ )

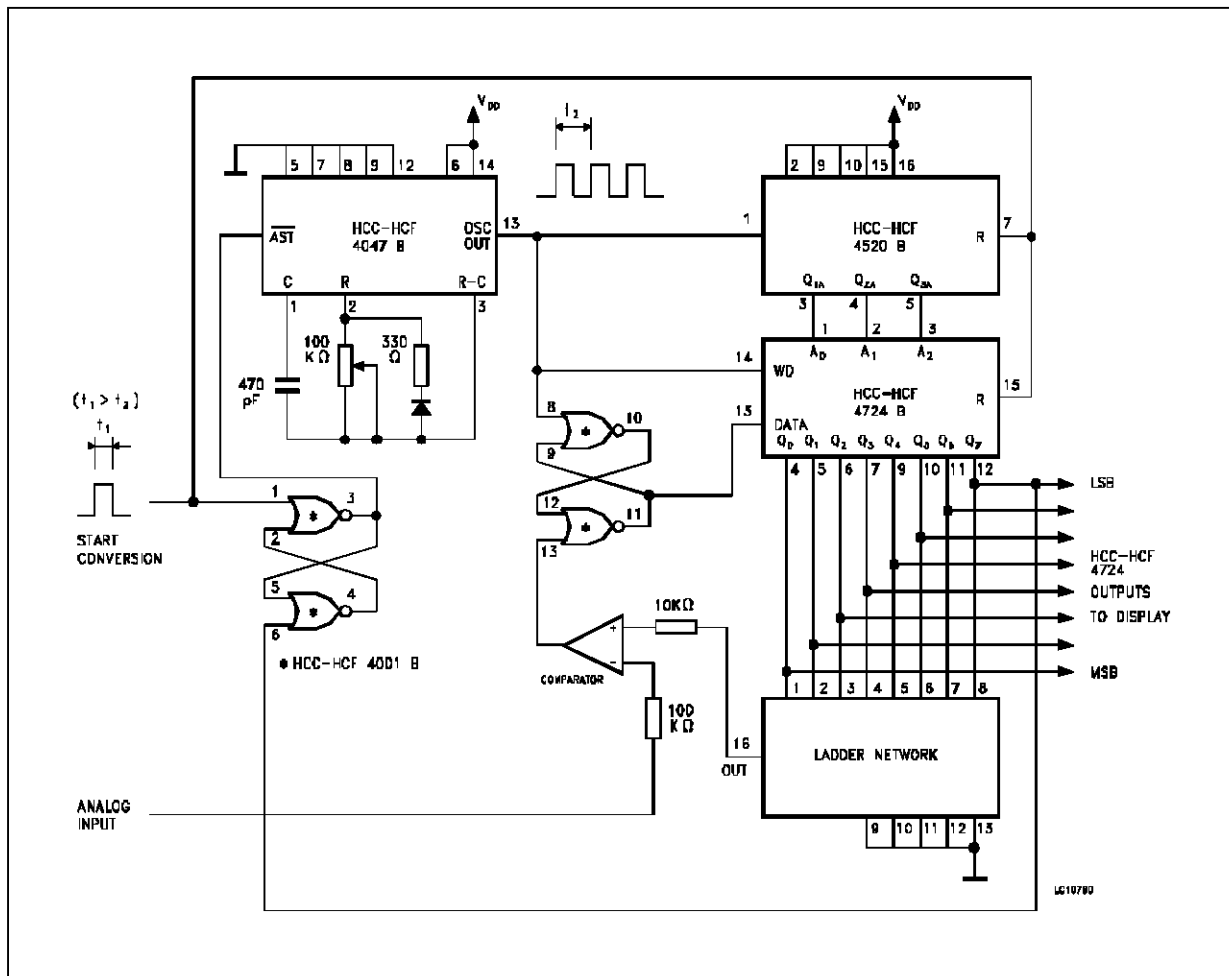
Symbol	Parameter	Test Conditions	Value			Unit	
			$V_{DD}$ (V)	Min.	Typ.		Max.
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Data to Output	(See Figure 1)	5		200	400	ns
			10		75	150	
			15		50	100	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Write Disable to Output	(See Figure 1)	5		200	400	ns
			10		80	160	
			15		60	120	
$t_{PHL}$	Propagation Delay Time Reset to Output	(See Figure 1)	5		175	350	ns
			10		80	160	
			15		65	130	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Address to Output	(See Figure 1)	5		225	450	ns
			10		100	200	
			15		75	150	
$t_{TLH}$ $t_{THL}$	Transition Time Any Output		5		100	200	ns
			10		50	100	
			15		40	80	
$t_w$	Minimum Pulse Width Data	(See Figure 1)	5		100	200	ns
			10		50	100	
			15		40	80	
	Minimum Pulse Width Address	(See Figure 1)	5		200	400	ns
			10		100	200	
			15		65	125	
	Minimum Pulse Width Reset	(See Figure 1)	5		75	150	ns
			10		40	75	
			15		25	50	
$t_s$	Minimum Setup Time Data to Write Disable	(See Figure 1)	5		50	100	ns
			10		25	50	
			15		20	35	
$t_H$	Minimum Hold Time Data to Write Disable	(See Figure 1)	5		75	150	ns
			10		40	75	
			15		25	50	
$C_{IN}$	Input Capacitance		Any Input		5	7.5	pF

Figure 1: Master Timing Diagram

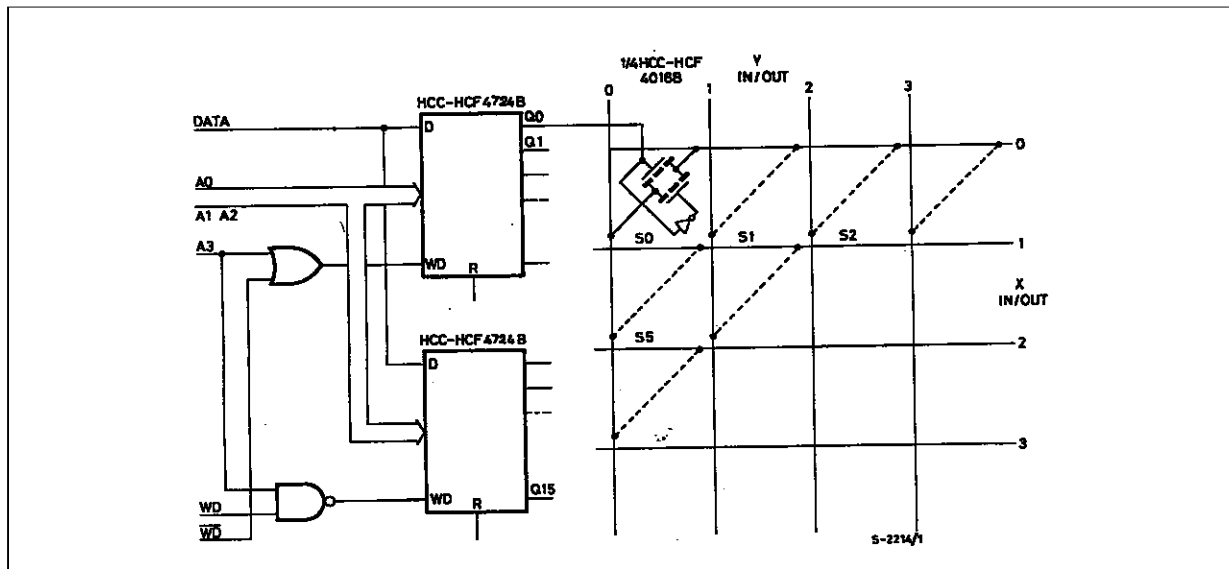


TYPICAL APPLICATIONS

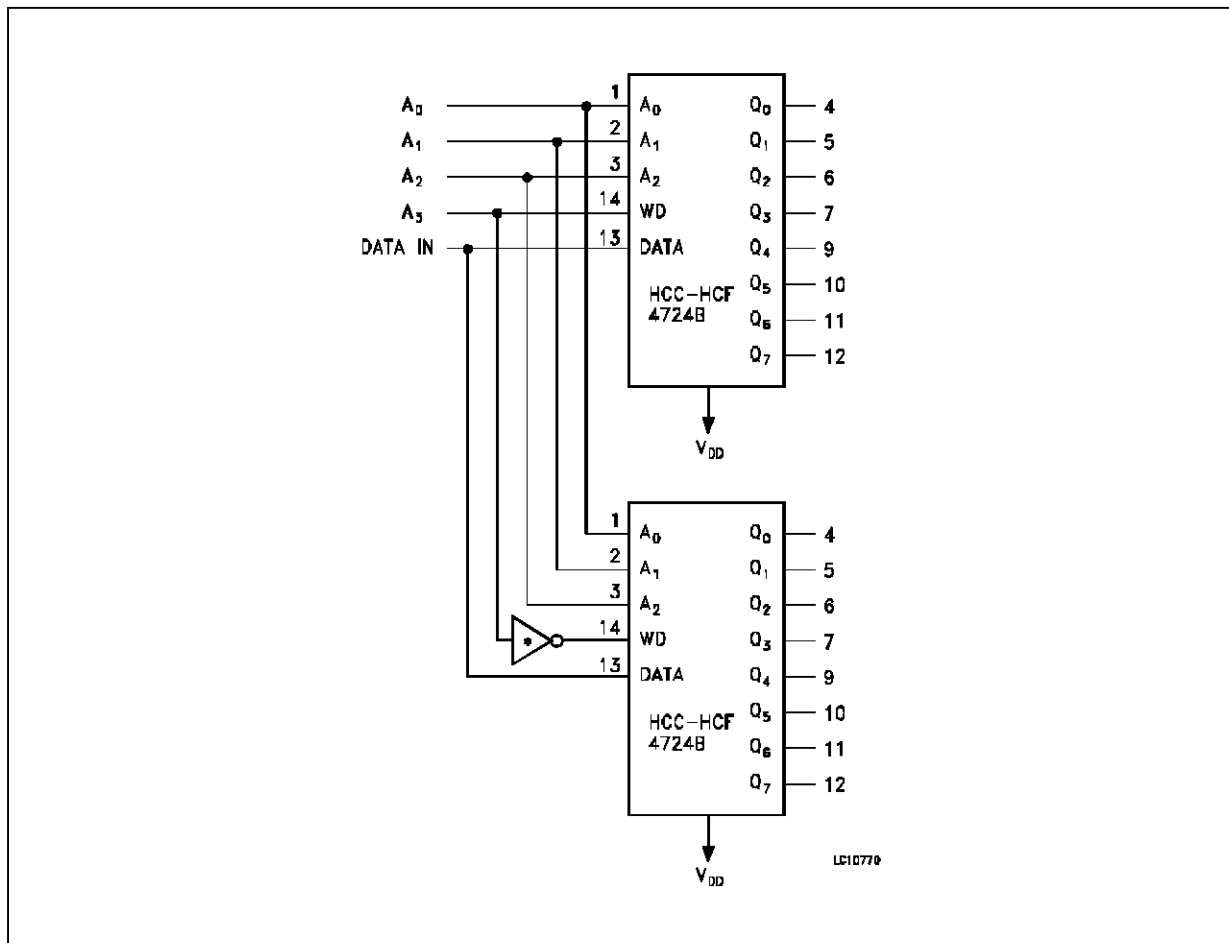
A/D Converter



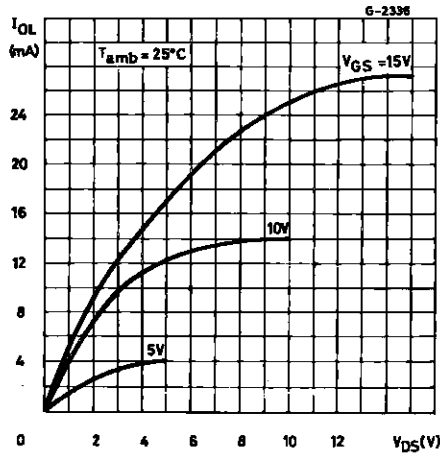
Multiple Selection Decoding - 4 x 4 Crosspoint Switch



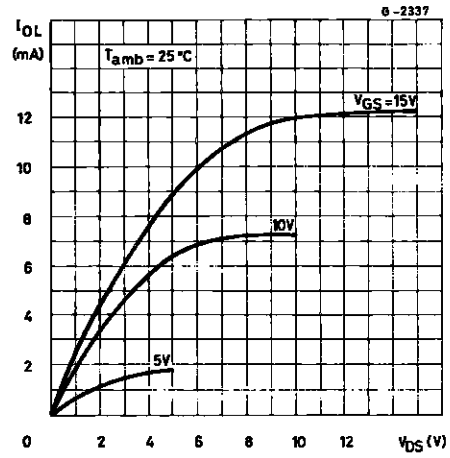
1 of 6 Decoder/Demultiplexer



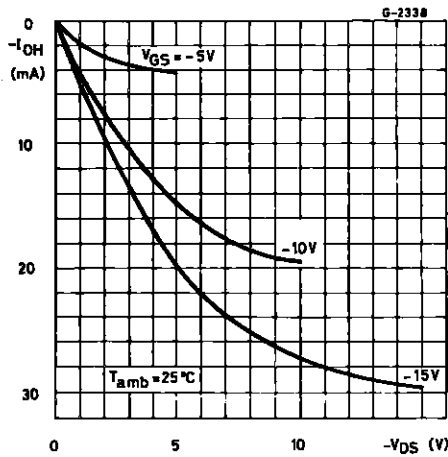
Typical Output Low (sink) Current Characteristics



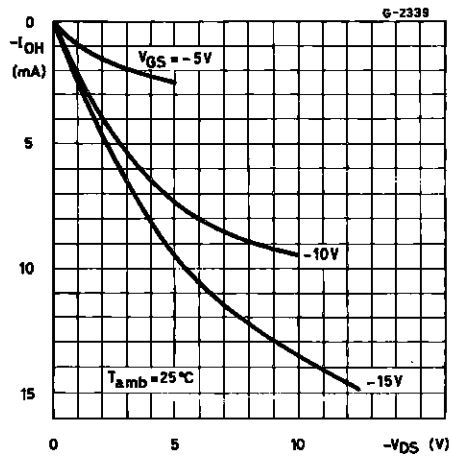
Minimum Output Low (sink) Current Characteristics



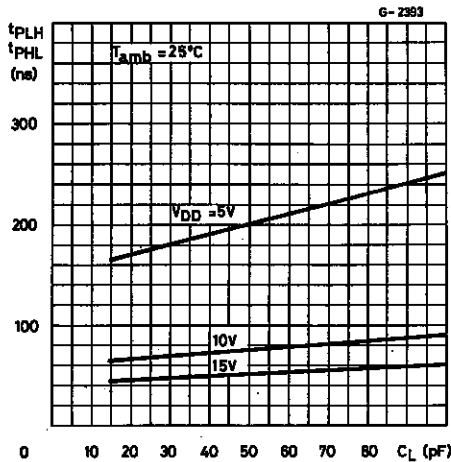
Typical Output High (source) Current Characteristics



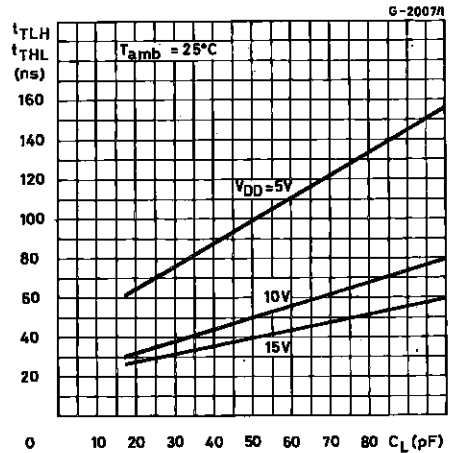
Minimum Output High (source) Current Characteristics



Typical Propagation Delay Time (data to Qn) vs Load Capacitance

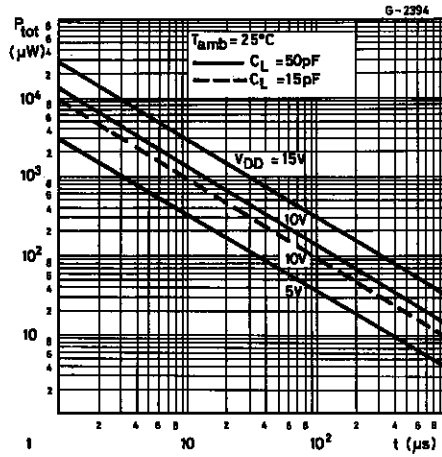


Typical Transition Time vs Load Capacitance



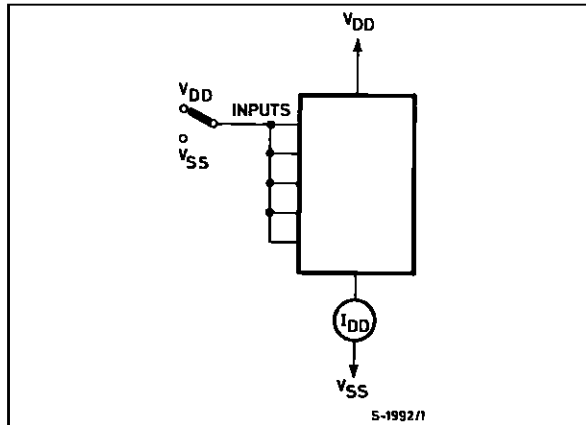


Typical Dynamic Power Dissipation vs Address Cycle Time

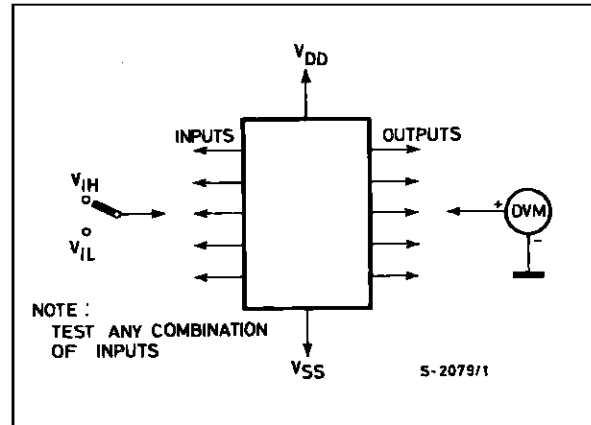


TEST CIRCUITS

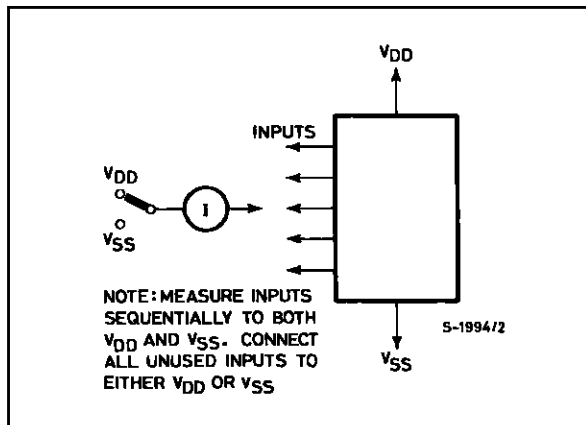
Quiescent Device Current



Noise Immunity



Input Leakage Current



**Plastic DIP16 (0.25) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

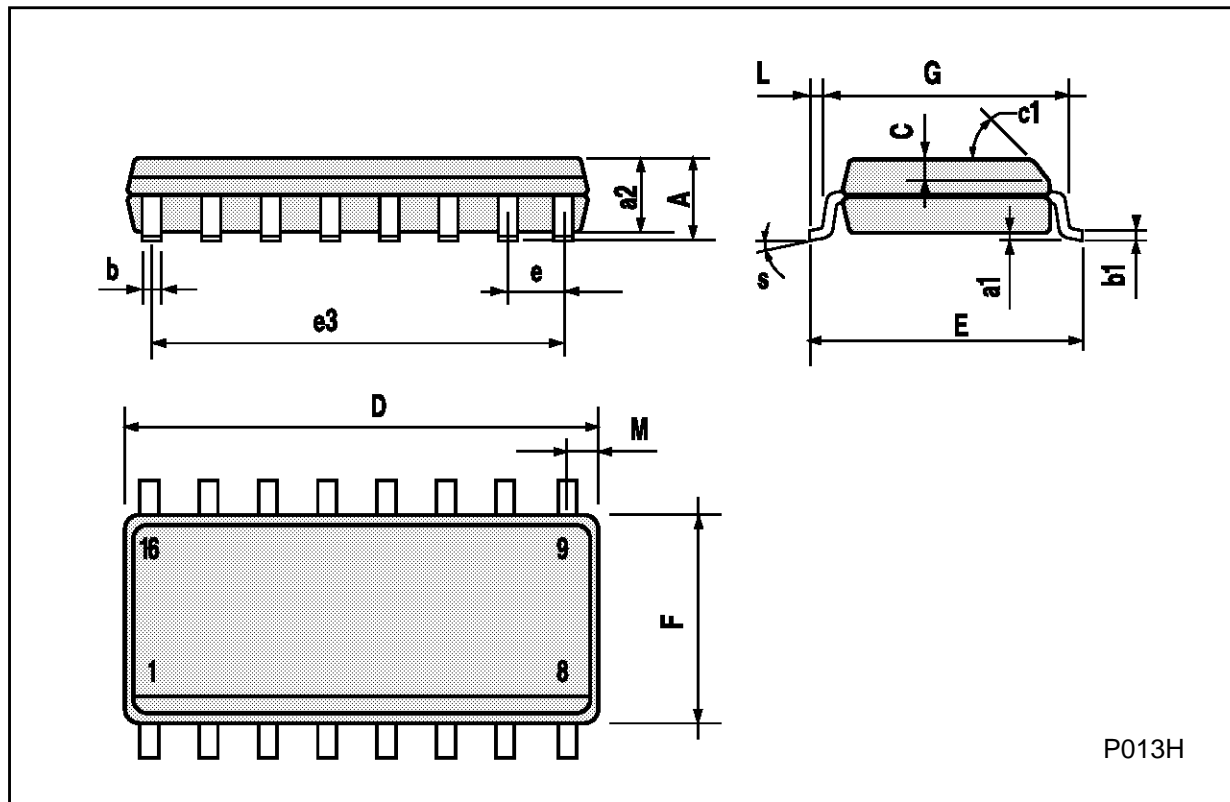
**Ceramic DIP16/1 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

## PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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