

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT354**

**8-input multiplexer/register with  
transparent latches; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-input multiplexer/register with transparent latches; 3-state

## 74HC/HCT354

### FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL

(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input ( $\overline{LE}$ ).

The transparent 8-bit data latches are enabled when the active LOW data enable input ( $\overline{E}$ ) is LOW. When the output enable input  $\overline{OE}_1 = \text{HIGH}$ ,  $\overline{OE}_2 = \text{HIGH}$  or  $\overline{OE}_3 = \text{LOW}$ , the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	D <sub>n</sub> , $\overline{E}$ to Y, $\overline{Y}$		20	22	ns
	S <sub>n</sub> , $\overline{LE}$ to Y, $\overline{Y}$		24	27	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

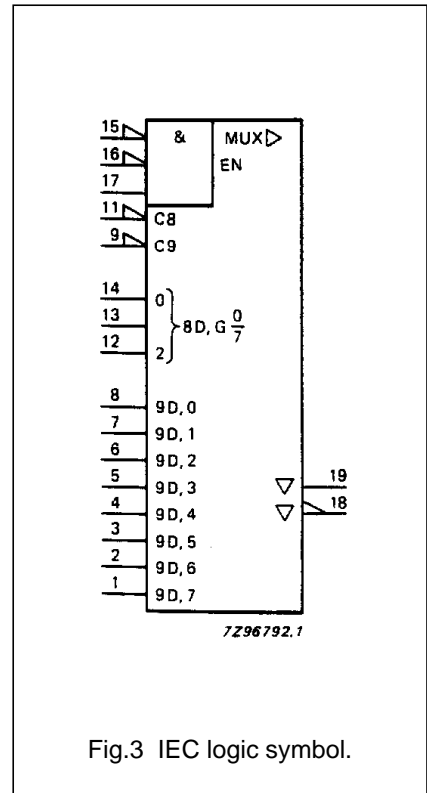
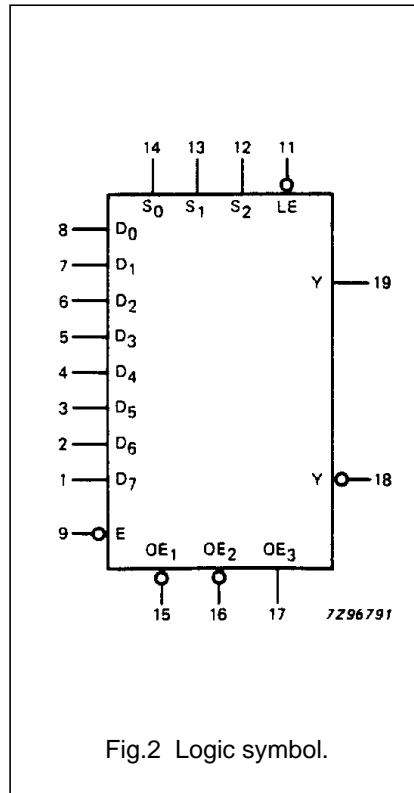
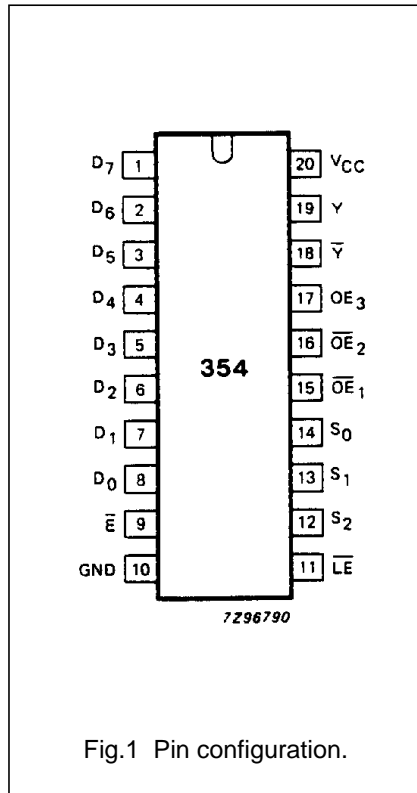
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 8-input multiplexer/register with transparent latches; 3-state

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D <sub>0</sub> to D <sub>7</sub>	data inputs
9	$\bar{E}$	data enable input (active LOW)
10	GND	ground (0 V)
11	$\bar{LE}$	address latch enable inputs (active LOW)
14, 13, 12	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	select inputs
15, 16	$\overline{OE}_1$ , $\overline{OE}_2$	output enable input (active LOW)
17	OE <sub>3</sub>	output enable input (active HIGH)
18	$\bar{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V <sub>CC</sub>	positive supply voltage



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FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS <sup>(1)</sup>			$\overline{E}$	OUTPUT ENABLE			Y	$\overline{Y}$	
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>		$\overline{OE}_1$	$\overline{OE}_2$	OE <sub>3</sub>			
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D <sub>0</sub>	$\overline{D}_0$	data latch is transparent
L	L	H	L	L	L	H	D <sub>1</sub>	$\overline{D}_1$	
L	H	L	L	L	L	H	D <sub>2</sub>	$\overline{D}_2$	
L	H	H	L	L	L	H	D <sub>3</sub>	$\overline{D}_3$	
H	L	L	L	L	L	H	D <sub>4</sub>	$\overline{D}_4$	
H	L	H	L	L	L	H	D <sub>5</sub>	$\overline{D}_5$	
H	H	L	L	L	L	H	D <sub>6</sub>	$\overline{D}_6$	
H	H	H	L	L	L	H	D <sub>7</sub>	$\overline{D}_7$	
L	L	L	H	L	L	H	D <sub>0n</sub>	$\overline{D}_{0n}$	data is latched
L	L	H	H	L	L	H	D <sub>1n</sub>	$\overline{D}_{1n}$	
L	H	L	H	L	L	H	D <sub>2n</sub>	$\overline{D}_{2n}$	
L	H	H	H	L	L	H	D <sub>3n</sub>	$\overline{D}_{3n}$	
H	L	L	H	L	L	H	D <sub>4n</sub>	$\overline{D}_{4n}$	
H	L	H	H	L	L	H	D <sub>5n</sub>	$\overline{D}_{5n}$	
H	H	L	H	L	L	H	D <sub>6n</sub>	$\overline{D}_{6n}$	
H	H	H	H	L	L	H	D <sub>7n</sub>	$\overline{D}_{7n}$	

## Notes

1. This column shows the input address set-up with  $\overline{LE} = \text{LOW}$  (address latch is transparent).
2. D<sub>0</sub> to D<sub>7</sub> = data at inputs D<sub>0</sub> to D<sub>7</sub>  
D<sub>0n</sub> to D<sub>7n</sub> = data at inputs D<sub>0</sub> to D<sub>7</sub> before the most recent LOW-to-HIGH transition of  $\overline{E}$   
H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

# 8-input multiplexer/register with transparent latches; 3-state

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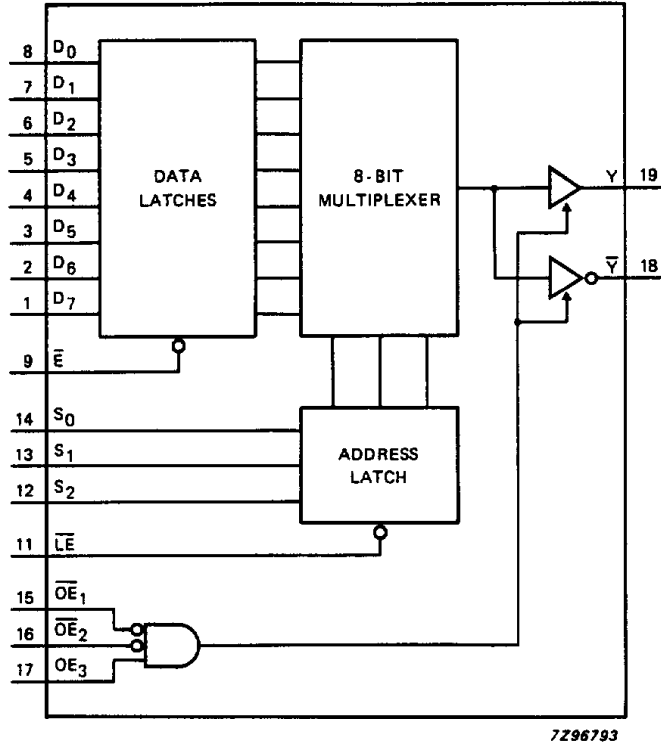


Fig.4 Functional diagram.

# 8-input multiplexer/register with transparent latches; 3-state

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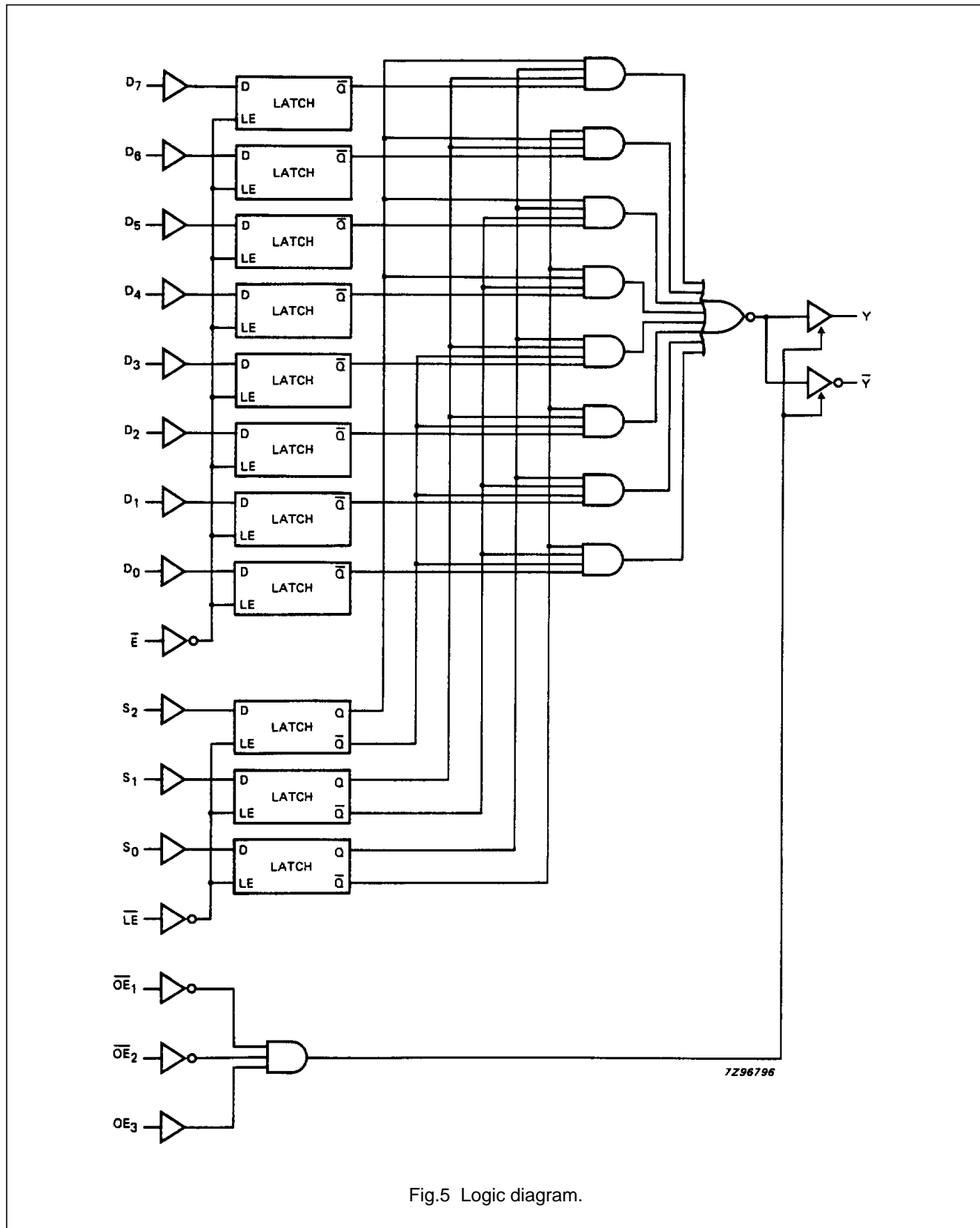


Fig.5 Logic diagram.

# 8-input multiplexer/register with transparent latches; 3-state

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Y, $\bar{Y}$		61 22 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to Y, $\bar{Y}$		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to Y, $\bar{Y}$		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{LE}$ to Y, $\bar{Y}$		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig.9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>n</sub> to Y, $\bar{Y}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.10
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>3</sub> to Y, $\bar{Y}$		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>n</sub> to Y, $\bar{Y}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>3</sub> to Y, $\bar{Y}$		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9
t <sub>w</sub>	data enable pulse width $\bar{E}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	latch enable pulse width $\bar{LE}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>su</sub>	set-up time D <sub>n</sub> to $\bar{E}$	50	11		65		75		ns	2.0 4.5 6.0	Fig.10	
t <sub>su</sub>	set-up time S <sub>n</sub> to $\bar{LE}$	50	14		65		75		ns	2.0 4.5 6.0	Fig.10	
t <sub>h</sub>	hold time D <sub>n</sub> to $\bar{E}$	5	-6		5		5		ns	2.0 4.5 6.0	Fig.11	
t <sub>h</sub>	hold time S <sub>n</sub> to $\bar{LE}$	5	-8		5		5		ns	2.0 4.5 6.0	Fig.10	



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**8-input multiplexer/register with  
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**74HC/HCT354****DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub> , S <sub>n</sub>	0.2
OE <sub>3</sub>	0.25
$\overline{LE}$	0.5
$\overline{E}$ , $\overline{OE}_n$	1.0

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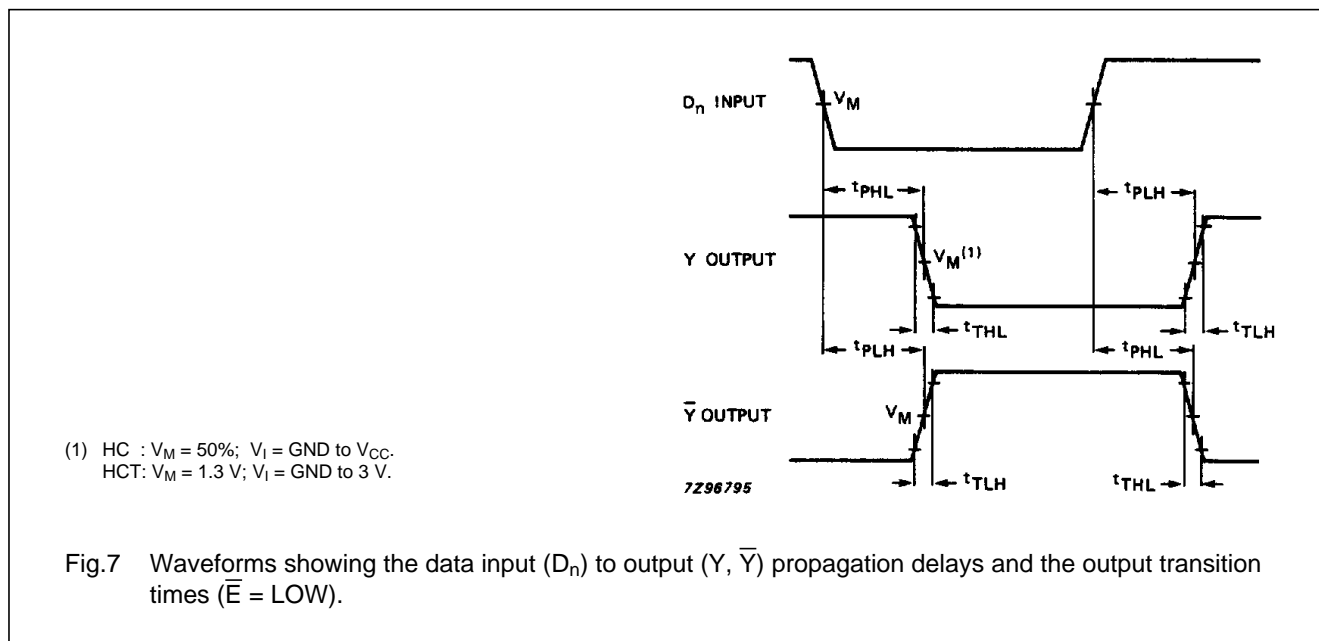
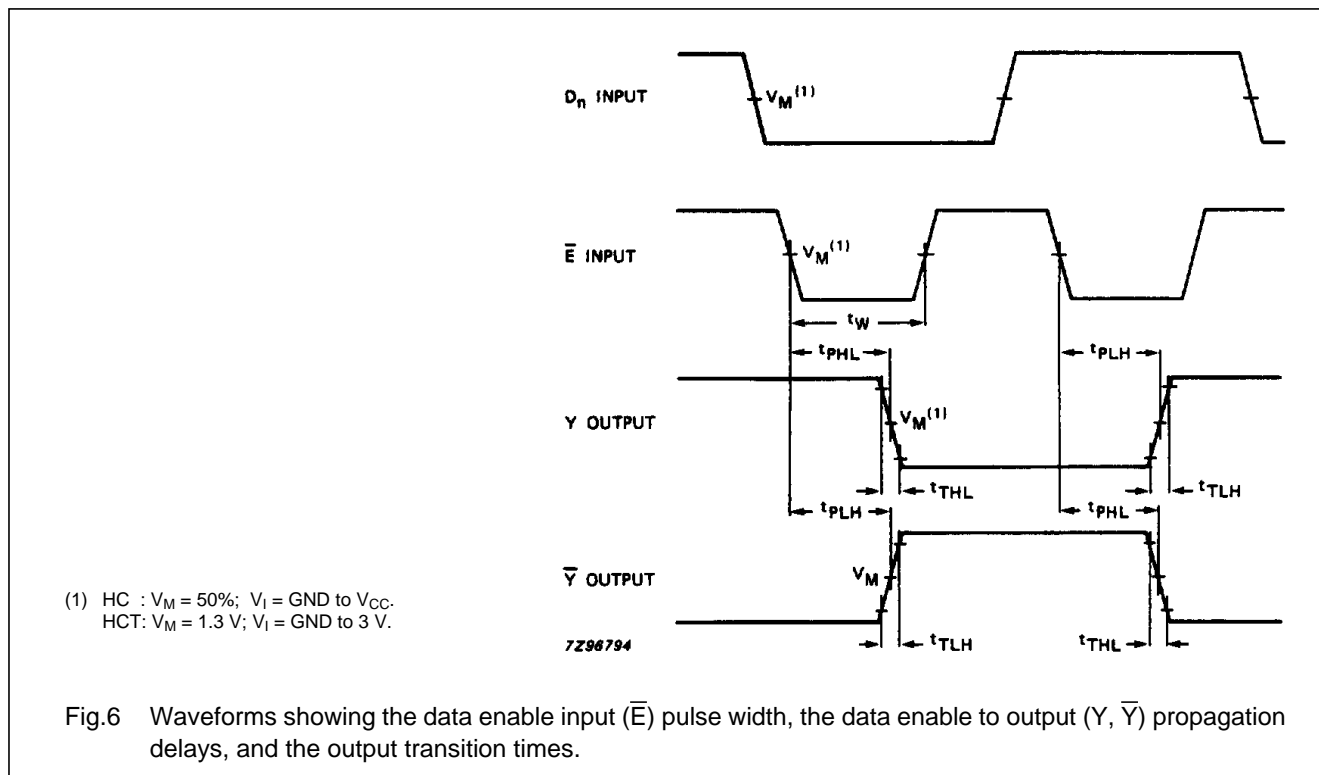
**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Y, \bar{Y}$		25	47		59		71	ns	4.5	Fig.7	
$t_{PHL}/t_{PLH}$	propagation delay $\bar{E}$ to $Y, \bar{Y}$		26	54		68		81	ns	4.5	Fig.6	
$t_{PHL}/t_{PLH}$	propagation delay $S_n$ to $Y, \bar{Y}$		30	59		74		89	ns	4.5	Fig.8	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{LE}$ to $Y, \bar{Y}$		31	63		79		95	ns	4.5	Fig.9	
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}_n$ to $Y, \bar{Y}$		18	34		43		51	ns	4.5	Fig.10	
$t_{PZH}/t_{PZL}$	3-state output enable time $OE_3$ to $Y, \bar{Y}$		18	34		43		51	ns	4.5	Fig.10	
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}_n$ to $Y, \bar{Y}$		18	33		41		50	ns	4.5	Fig.10	
$t_{PHZ}/t_{PLZ}$	3-state output disable time $OE_3$ to $Y, \bar{Y}$		21	39		49		59	ns	4.5	Fig.10	
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9	
$t_W$	data enable pulse width $\bar{E}$ LOW	16	6		20		24		ns	4.5	Fig.6	
$t_W$	latch enable pulse width $\overline{LE}$ LOW	16	6		20		24		ns	4.5	Fig.9	
$t_{su}$	set-up time $D_n$ to $\bar{E}$	10	4		13		15		ns	4.5	Fig.11	
$t_{su}$	set-up time $S_n$ to $\overline{LE}$	10	5		13		15		ns	4.5	Fig.10	
$t_h$	hold time $D_n$ to $\bar{E}$	9	0		11		14		ns	4.5	Fig.11	
$t_h$	hold time $S_n$ to $\overline{LE}$	9	-3		11		14		ns	4.5	Fig.10	

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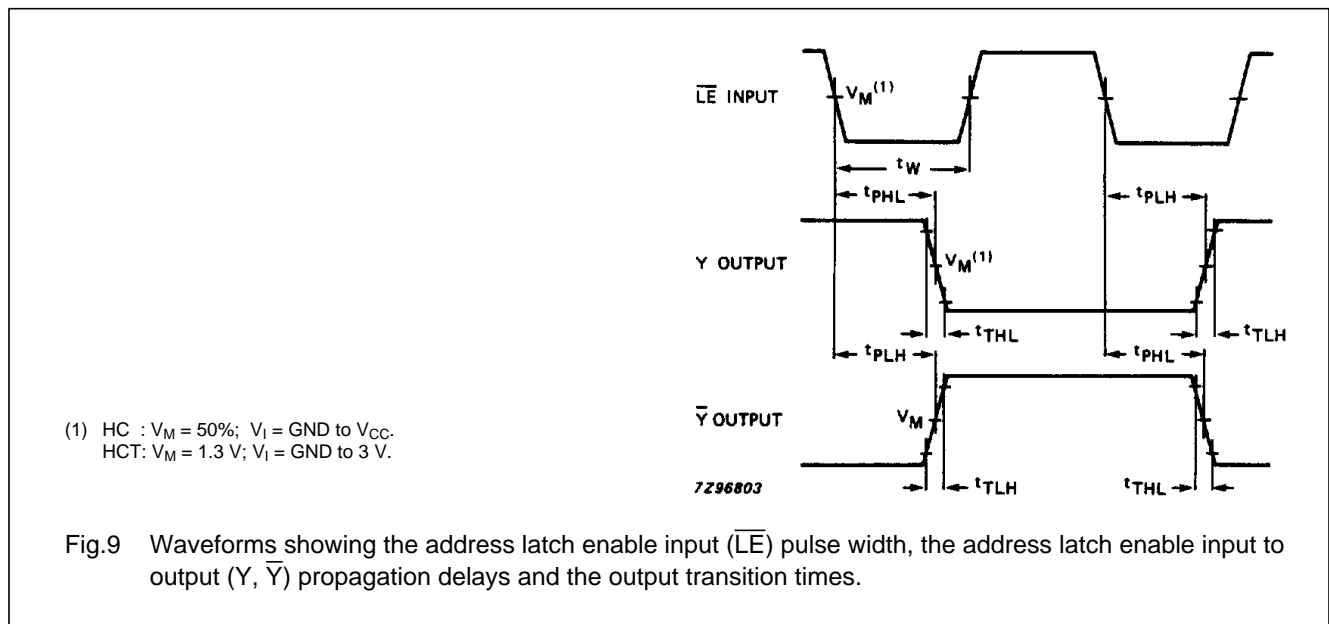
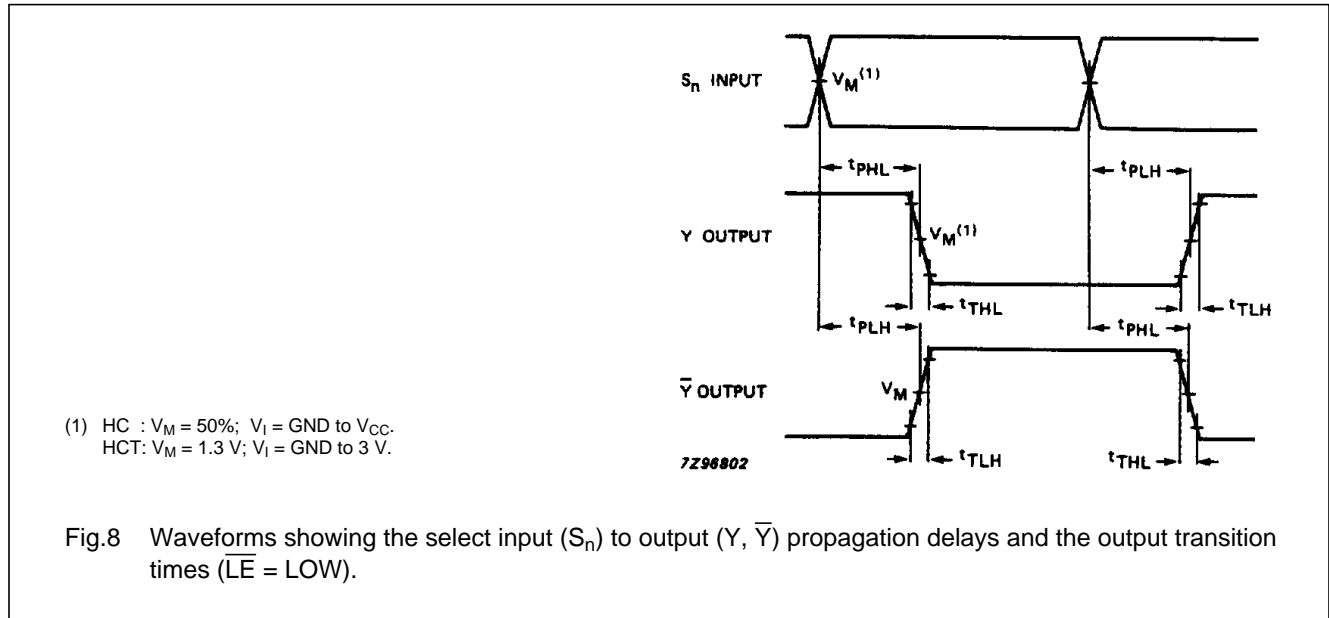
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AC WAVEFORMS



8-input multiplexer/register with transparent latches; 3-state

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# 8-input multiplexer/register with transparent latches; 3-state

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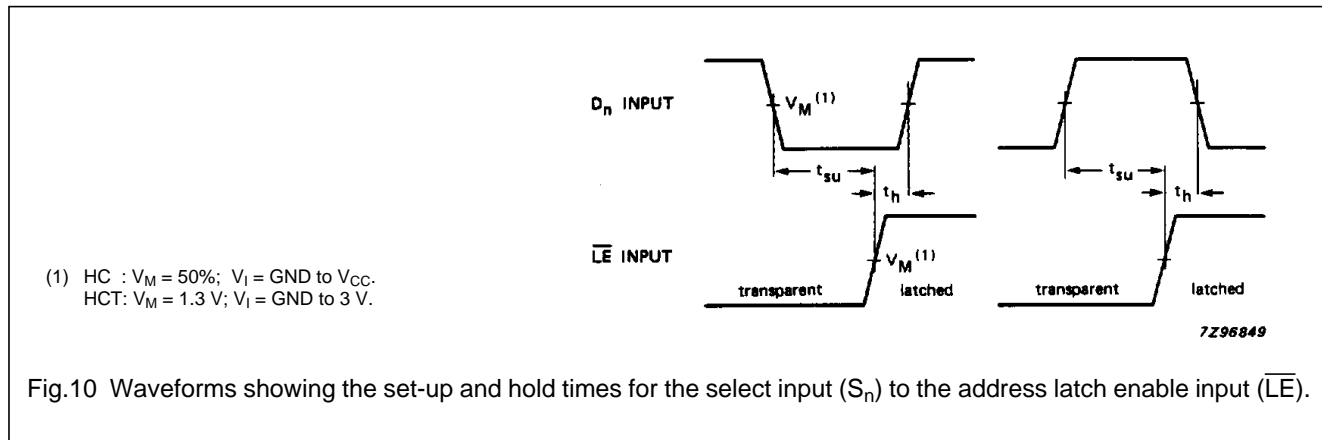


Fig.10 Waveforms showing the set-up and hold times for the select input ( $S_n$ ) to the address latch enable input ( $\overline{LE}$ ).

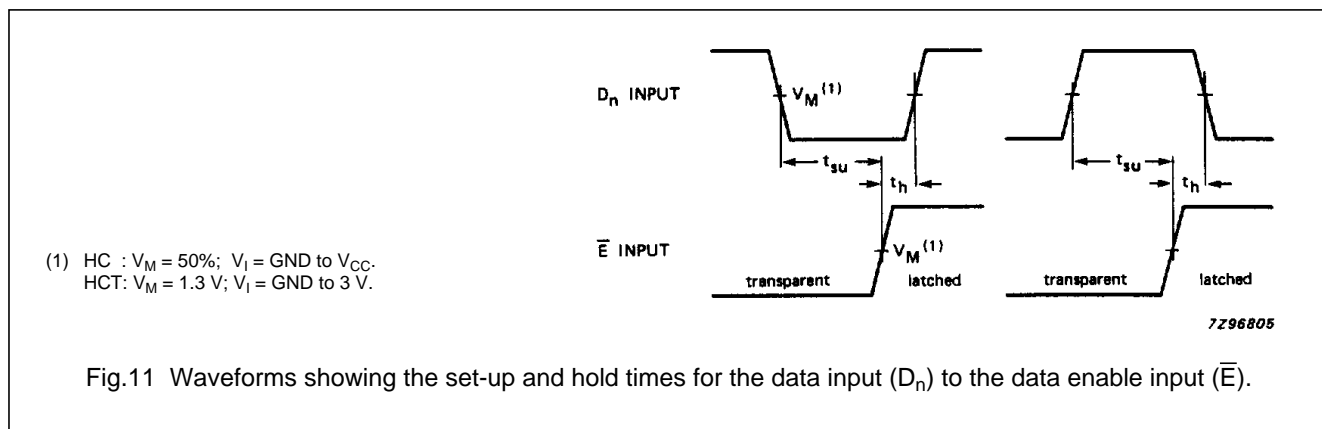


Fig.11 Waveforms showing the set-up and hold times for the data input ( $D_n$ ) to the data enable input ( $\overline{E}$ ).

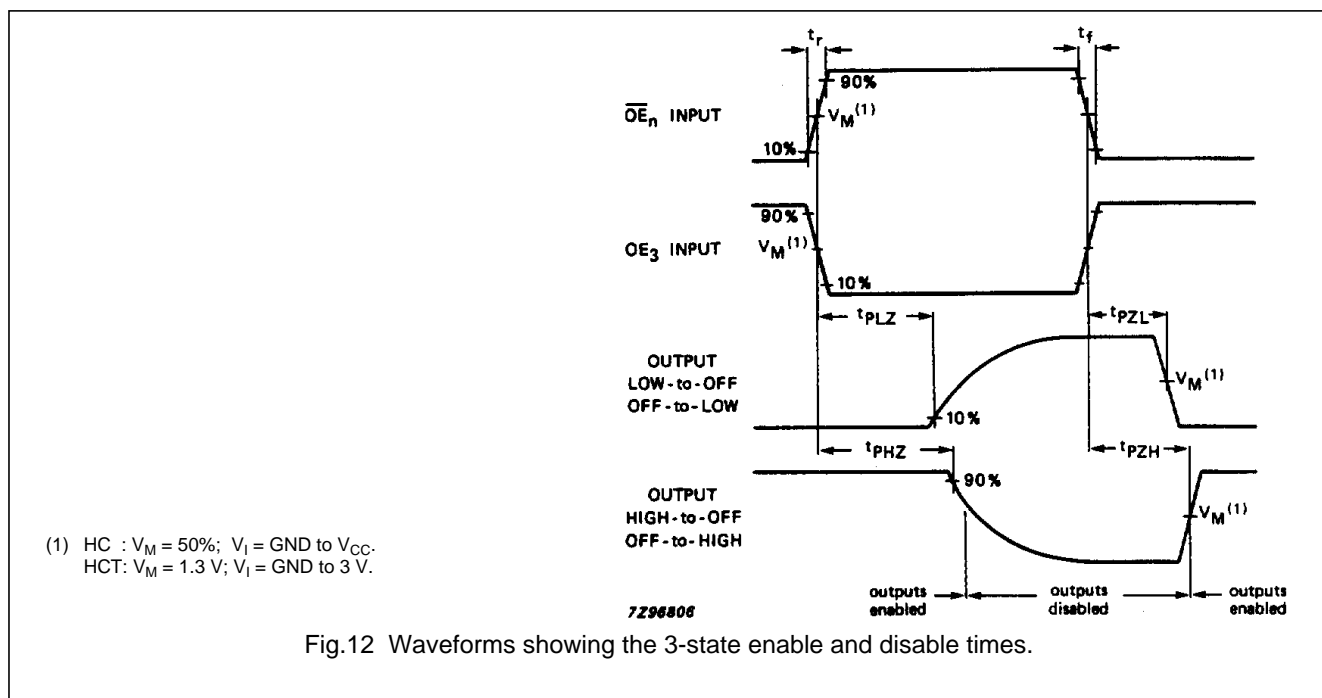


Fig.12 Waveforms showing the 3-state enable and disable times.

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8-input multiplexer/register with  
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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.